Crystal Oscillator

This application note addresses issues commonly raised during the selection of the reference crystal, typically 14.318 MHz, for Chrontel's product line.

Pierce Oscillator

A simplified schematic of the oscillator circuit used in Chrontel products is shown in **Figure 1**. Note that the typical 2-pin crystal has been replaced by its equivalent circuit model.

- **Co** is the pin-to-pin capacitance. Its value is associated with the crystal electrode design and the crystal holder.
- **Rs** is the motion resistance. Its value is specified by the crystal manufacturer.
- **Cs** is the motion capacitance and **Ls** is the motion inductance, which are not specified, and are functions of the crystal frequency.
- **Rbias** is a feedback resistor, implemented on-chip in Chrontel products, which provides DC bias to the inverting amplifier.
- **C1** and **C2** are total capacitance-to-ground at the input and output nodes of the amplifier, respectively. If external capacitance is not added, the values of the internal capacitance C1 and C2, including pin parasitic capacitance, are each approximately 15pF to 20pF.

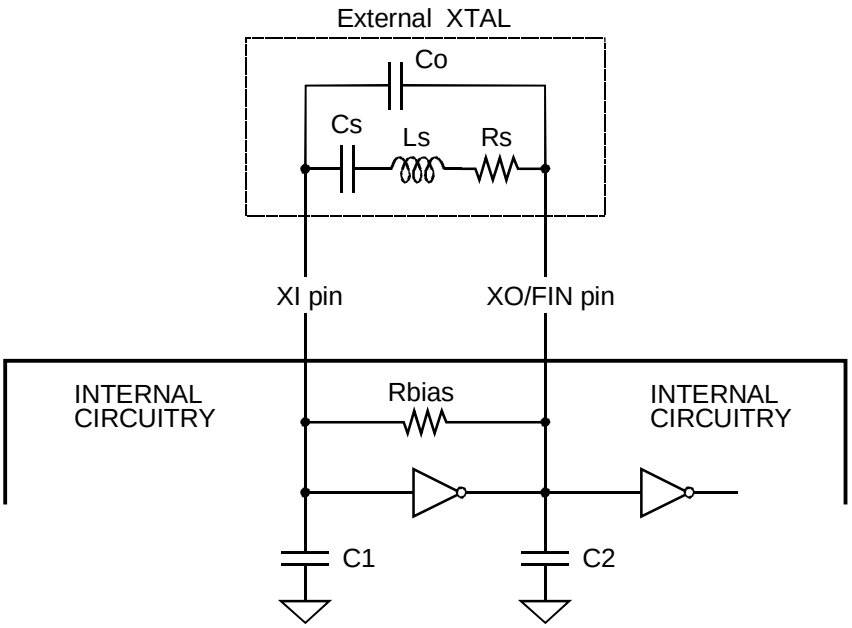

Figure 1: Pierce Oscillator

Crystal Specifications

The reference frequencies for Chrontel's products are derived from an on-chip Pierce oscillator with an external crystal. The oscillator has been designed to function reliably with crystals that conform to the following specifications:

Table 1 • Crystal Specifications

Crystal Specifications	Min	Typical	Max	Comment
Nominal Frequency (MHz)		14.31818		
Oscillation Mode		Fundamental		
Holder Type		HC-49, HC-50		Not Important
Pin to Pin Capacitance (Co in pF)		7	10	Depends on Holder Type
Operating Temperature (°C)	–10	30	70	Application Dependent
Frequency Tolerance		± 30PPM		Application Dependent
Load Capacitance (Ceq in pF)	12.5	17	20	Affects Frequency Tolerance
Drive Level (P in μW)	0.5	1	2*	Calc. Value by (4)
Motion Resistance (Rs in Ω)	25	30	50	Affects Drive Level

* Drive level must be higher than the calculated power dissipation of the crystal as given by (4).

Series and Parallel Resonance

There is no such thing as a “series cut” crystal as opposed to a “parallel cut” crystal. The same crystal can be made to oscillate in series resonance mode or parallel resonance mode. The frequency of oscillation of a crystal is usually specified by the manufacturer as either the series resonance frequency or the parallel resonance frequency. A crystal can oscillate in series resonance, meaning that Ls is resonating with Cs, and the resonance frequency is then simply

$$fseries = \frac{1}{2\pi\sqrt{Ls \times Cs}} \quad (1)$$

Some oscillator circuits are designed for series resonance and the oscillation frequency shall equal the specified series resonance value. These series mode oscillators, however, are more sensitive to temperature and component variations. In fact, most crystals oscillators in today's ICs are of the parallel resonance type. The oscillation frequency of a parallel mode oscillator is always higher than *fseries*. The actual oscillation frequency of a parallel mode oscillator is dependent on the equivalent capacitance seen by the crystal.

$$fparallel = fseries\left(1 + \frac{Cs}{2Ceq}\right) \quad (2)$$

where

$$Ceq = Co + C1\left(\frac{C2}{C1 + C2}\right) \quad (3)$$

At parallel resonance, the crystal behaves inductively and resonates with capacitance shunting the crystal terminals. Depending on the application, especially in microprocessors where Pierce oscillators are used predominantly, a crystal manufacturer may specify parallel resonance frequency instead of series resonance frequency. Since *fparallel* is a function of the load capacitance Ceq, it should also be specified along with *fparallel*.

For PC CPU clock and VGA clock applications, the frequency accuracy required is usually not very stringent and can easily be satisfied with a 14.318 MHz crystal that has been specified for operation in either series or parallel resonance modes.

Crystal Power Dissipation

This is one of the more important specifications for a crystal. In operation, if the power dissipated in the crystal exceeds the specified drive level, the crystal may have long term reliability problems. The oscillation frequency may shift from the desired value, and in extreme cases the crystal may crack and stop oscillating altogether. For the circuit in **Figure 1**, crystal dissipation is given by

$$P \approx \frac{1}{2}(2\pi \times fparallel \times Ceq \times V)^2 \times Rs \quad (4)$$

Using typical values for Rs, Ceq and V equals 5V, P equals approximately 876 µW.

Since increasing the value of C1 and C2 would result in increased power dissipation in the crystal, it is not recommended that extra capacitance be added to pins XTAL1 and XTAL2 of the clock chip unless it is absolutely necessary to tune the frequency to a desired value. In the case that additional capacitances are added, a crystal with a higher drive level should be chosen according to the above equation.

Pullability and Cs

Most crystal manufacturers do not specify Cs explicitly. However, one can measure Cs indirectly by measuring the change in frequency for a given change in load capacitance. Cs is related to the crystal pullability by the following equation.

$$Pullability\ (ppm/pF) = \frac{Cs \times 10^6}{2 \times (Ceq)^2} \quad (5)$$

One can reduce the frequency of oscillation by adding external capacitance to C1 and C2 in equal amounts. The oscillation frequency is given by equation 2. Again, by increasing the value of C1 and C2, power dissipation of the crystal increases according to (4).

Oscillator Startup Time and PLL Lock Time

Oscillator start-up time is primarily a function of the size of the inverting amplifier. Measured oscillator start-up time is about 1 ms for Chrontel's clock chips.

PLL lock time is a function of the PLL unity gain frequency and the frequency spanned in the measurement. Lock time for Chrontel's PLL with internal loop filter is typically in the range of 5 to 20 ms for frequency to span from 0 Hz to 100 MHz. PLLs with external loop filters will have a longer lock time, depending on the external filter capacitor value.

By adding the oscillator start-up time and PLL lock time, Chrontel's clock chips typically reach their final stable frequency in less than 20 ms. In PC applications, this total start-up time is much less than the time required for the system to reach "Power Good," which is well over 100 ms.

REFERENCES

Intel Application Note AP-155, *Oscillators for Microcontrollers*, 1983.

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