PCB Layout and design Considerations for CH7007 and CH7008

Introduction

This application note focuses on the basic PCB layout and design guidelines for the CH7007 and CH7008 VGA-to-TV encoder products. Guidelines in component placement, power supply decoupling, grounding, and reference crystal placement and selection, input signal interface and video output component are discussed in this document. The guidelines discussed here are intended to optimize the PCB layout and application for these products. These are only recommendations. Designers are urged to implement the configurations and evaluate the performance of the system prior to bringing the design to production.

The discussion and figures that follow reflect and describe connections based on the 44-pin PLCC package. Users are urged to consult the CH7007/CH7008 datasheets for the pin assignments of the corresponding signals in the TQFP packages offered.

Component Placement

Components associated with the CH7007/CH7008 encoders should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

• Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1µF ceramic capacitor to each of the power supply pins as shown in **Figure 1** and **Figure 3**. These capacitors (C1 - C6, C15 and C16) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7007/CH7008 ground pins, in addition to ground vias.

• Ground Pins

The analog and digital grounds of the CH7007/CH7008 should connect to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7007/ CH7008 ground pins should connect directly to its respective decoupling capacitor ground lead, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance.

• Power Supply Pins

Separate digital (including the I/O supply voltage DVDD2), analog, and DAC power planes are recommended. Digital power should be supplied to pins 11, 22 and 36 (DVDD); I/O supply voltage should be applied to pin 44 (DVDD2); analog power should be supplied to pin 37 (AVDD); and DAC power should be supplied to pin 31 (VDD). The analog and DAC supplies are connected to a single +5V supply through ferrite beads, as shown in the schematic on **Figure 1**. The digital supplies are provided by the +3.3V supply and 1.8V to 3.3V supply (DVDD2) used by the graphic controller directly, depending on the logic level of the input pixel data.

A positive 5V regulator may be used if a clean +5V supplies are not available. Please refer to **Figure 2** for the optional positive 5V regulator circuits.

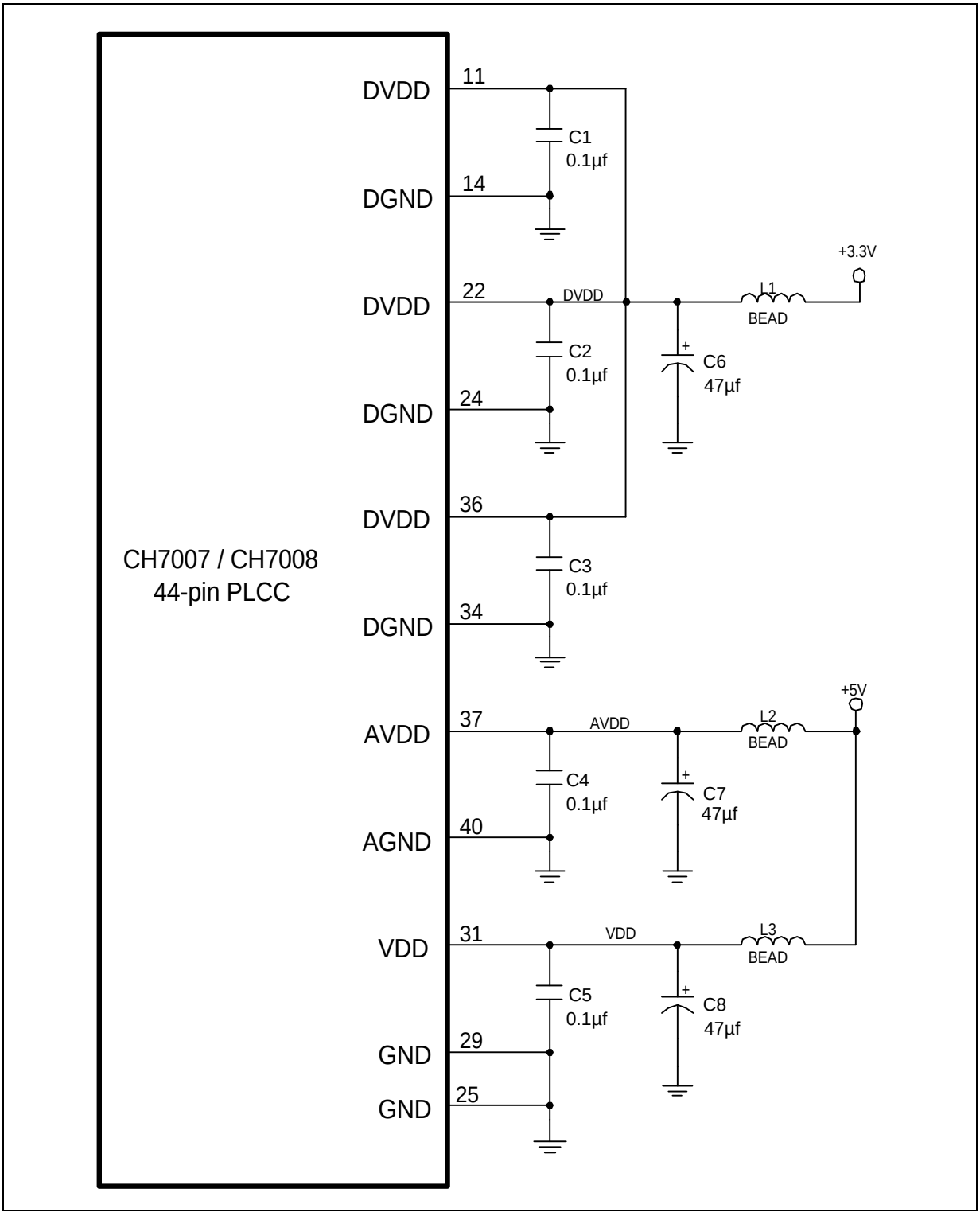

Figure 1: Power Supply Decoupling and Distribution

Notes: All the Ferrite BEAD decribed in this document is recommended to have < .05Ω @ DC; 23Ω @ 25MHz & 47Ω @ 100MHz. Please refer to Fair_Rite part# 2743019447 for detail or an equivanlent part can be used for the design.

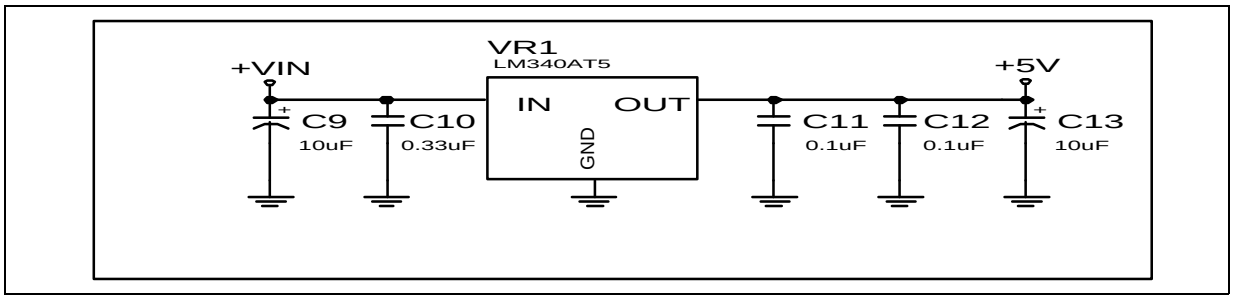

Figure 2: Optional Positive 5V Voltage Regulator

Note: Depends on the regulator used, there is a minimum voltage requirement for the VIN in order to achieve regulated +5V. Please refer the regulator data sheet for the requirement.

- **DVDD2 & VREF decoupling and connection**

VREF is used as a reference level for pixel data input D[11:0], H sync input, V sync input, P-OUT output. For the optimum decoupling, please refer **Figure 3**.

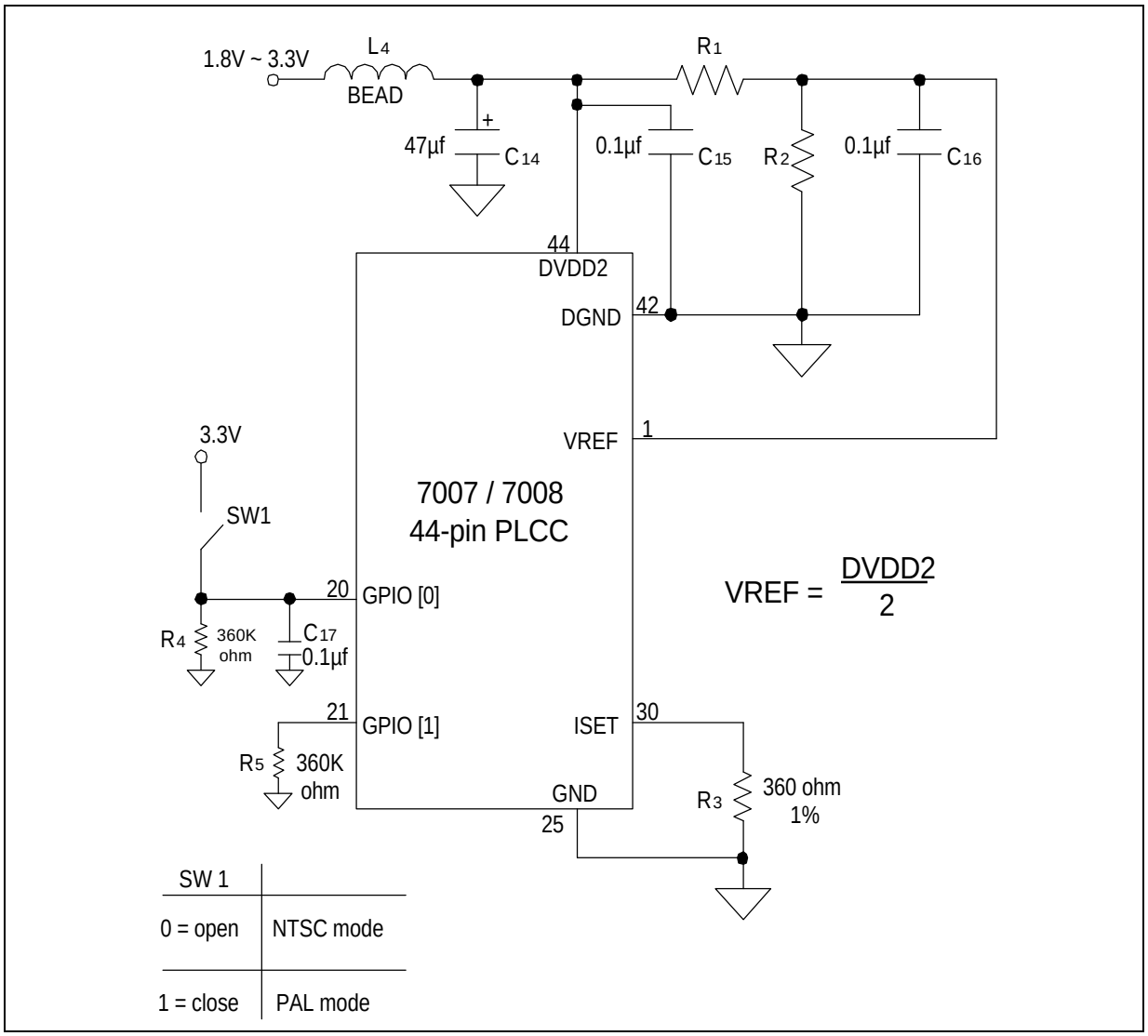

Figure 3: ISET reference voltage and DVDD2 connection

In general application, VREF is derived from DVDD2 divided by 2. (Therefore, both resistors value showed the same value; i.e. 10KΩ @ 1%. The decoupling capacitor is required as shown in **Figure 3**). Also the DVDD2 voltage supply should be conneted to the graphic controller I/O VDD which must be within 1.8V to 3.3V supply range (matches the output drive level from the graphic controller).

- **ISET pin**

A 360Ω resistor should be placed directly and as close as possible to pin 30 with short and wide traces. Whenever possible, the ISET resistor's ground pin should also be connected to the pin 25. Otherwise, the ground reference of the ISET resistor should ideally be close to the CH7007/CH7008.

- **GPIO [0] & GPIO [1]**

In applications using Intel 752 graphic accelerator & Intel 810 chipset* and the Intel software driver, it is recommended that the pins should be configured as shown in **Figure 3**.

Horizontal and Vertical Sync Signals

In input modes where the horizontal and vertical sync signals from the graphics controller are shared between the CH7007/CH7008 and the computer monitor, buffering the sync signals prior to connecting them to the monitor is recommended (please refer to **Figure 4** below). These buffers help isolate any noise generated from the monitor connection (e.g., reflections, etc.) from coupling into the sync inputs of the CH7007/CH7008, thereby degrading the display quality. In modes where the embedded syncs are used, these buffers are not necessary.

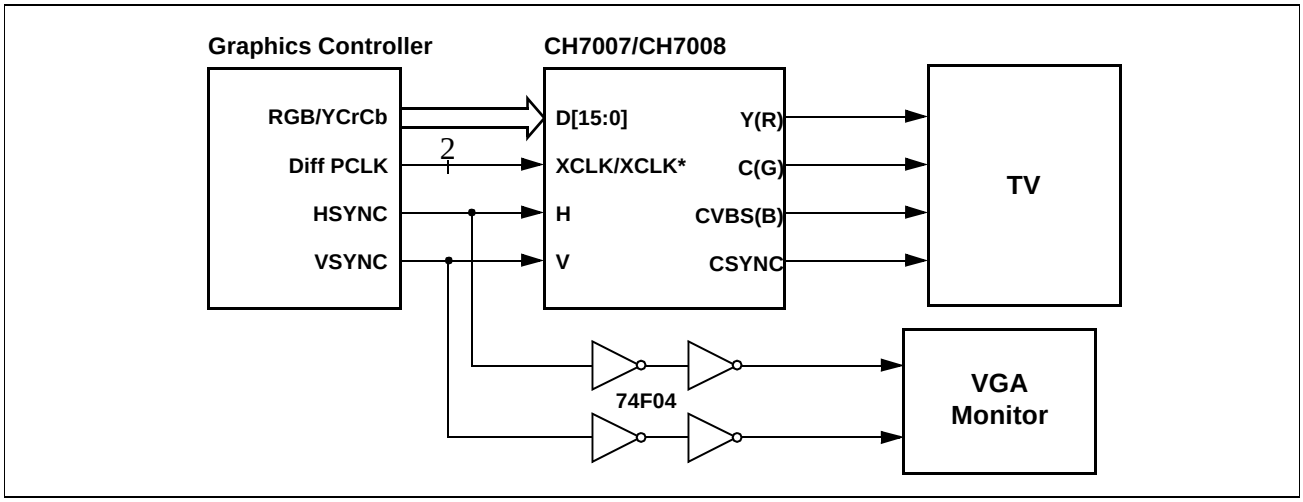

Figure 4: Sync Buffers

Note: If differential pixel clock from the graphic controller is not available, XCLK* should be tied to VREF.

Video Inputs

Since the digital pixel data and the pixel clock of the CH7007/CH7008 may toggle at speeds up to 100MHz (depending on input mode), it is critical that the connection of these signals between the graphics controller and the CH7007/CH7008 be kept short and isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals. Damping each line with a series resistor (30Ω-300Ω) will help minimize ringing on these lines.

Pixel Clock Mode

Depending on the architecture and configuration of the graphic controller, CH7007/CH7008 can be used in 5 different setting. In all these modes, H sync, V sync and pixel data D[11:0] must meet the setup and hold time with respective to pixel clock.

• Master Clock Mode (Figure 5)

P-OUT pin outputs a pixel clock to the graphic controller. The direction of H sync and V sync signal can be controlled by Sync Register 0DH. When the bit2 (SYO) = 0, the H sync and V sync signals are input to CH7007/CH7008. When the bit2 (SYO) = 1, the H sync and V sync signals are output to graphic controller. It is recommended to configure CH7007/8 in this clock mode with bit 2 of SR register set to 0 when the application use with the Intel 752 graphic accelerator and Intel 810 chipset.*

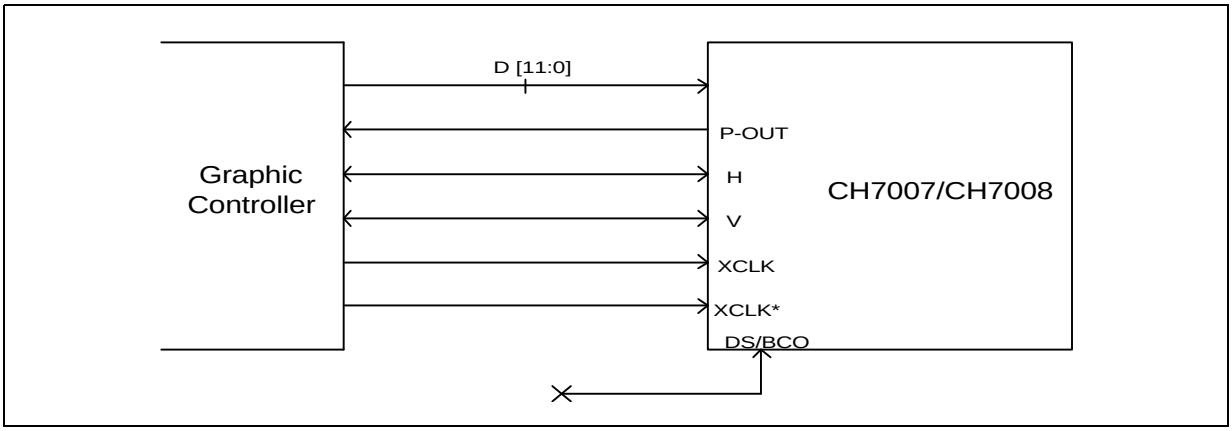

Figure 5 : Master Clock Mode

DS/BCO Pin

When DS/BCO is selected as an input, the rising edge of DS/BCO pin is used to signify the 1st active pixel for each active line. In applications using Intel 752 graphic accelerator & Intel 810 chipset* and the Intel software driver, it is recommended that the pin is not used, meaning that the pin is not connected to graphic controller at all. The active data start can use SAV register to set the number of pixels from the leading edge of H sync to the 1st active pixel with register 1CH bit4 = 0 and bit5 = 0.

• Slave Clock Mode (Figure 6)

For this mode, select register 06H bit 6 = 0. The pixel clock comes from the graphic controller and the P-OUT pin is in high impedance state. The direction of H sync and V sync signal can be controlled by the Sync Register 0DH. The same setting described under Master Clock Mode for the bit 2 (SYO) is applied here.

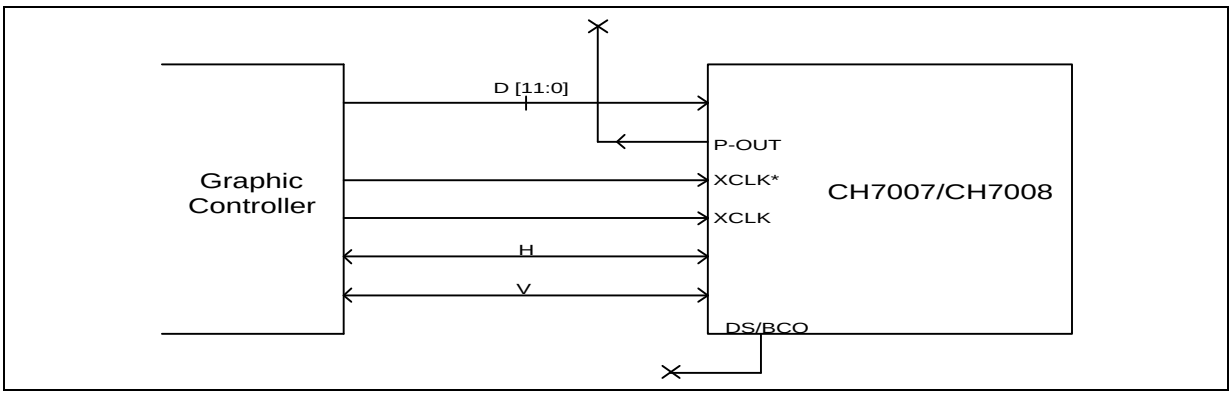

Figure 6 : Slave Clock Mode

- **Embedded Sync Mode (Figure 7)**

In order to enable this mode, register 04H needs to be set for IDF = 9. Since H sync and V sync signals can be embedded into the data stream, the connection of H sync and V sync pins are not required between the graphic controller and CH7007/CH7008. Please refer CCIR656 for details on how the H sync and V sync, odd field & even field signals are generated within the data stream.

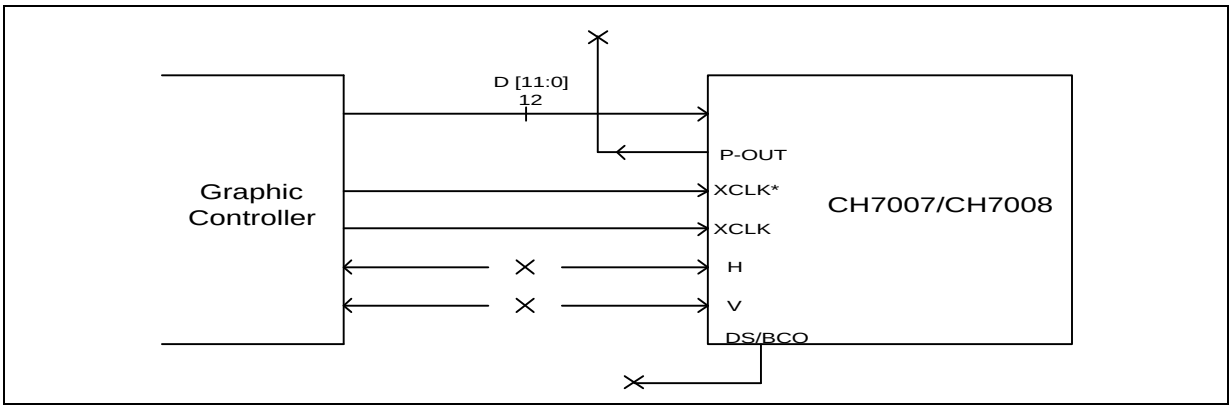

Figure 7: Embedded Sync Mode

Video Outputs

The components associated with the video output pins should be placed as close as possible to the CH7007/CH7008. The 75Ω output termination, the output filter network, and the output connectors should be located as close as possible to the CH7007/CH7008 to minimize the noise pickup as well as possible reflections due to impedance mismatches. The video output signals should overlay the ground plane and should be routed away from digital lines that could introduce crosstalk. The Y and C outputs should be separated by a ground trace and inductors and ferrite beads in series with these outputs should not be located next to each other.

The recommended output reconstruction filter network is a fourth order low pass filter. The recommended frequency response and the circuit elements are shown below.

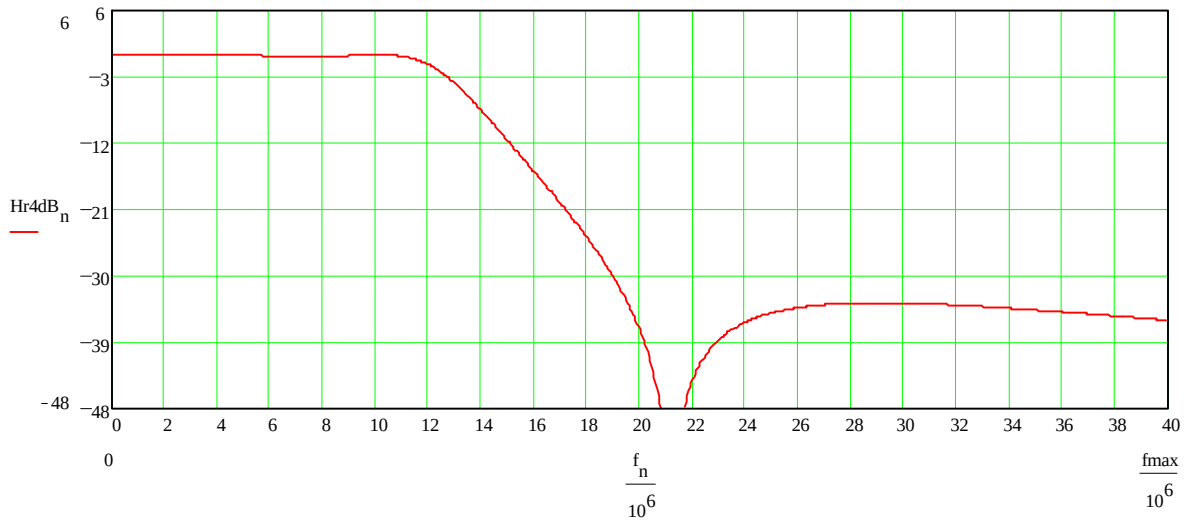

Figure 8: Amplitude response of 4th order reconstruction filter

Reconstruction filter (continued)

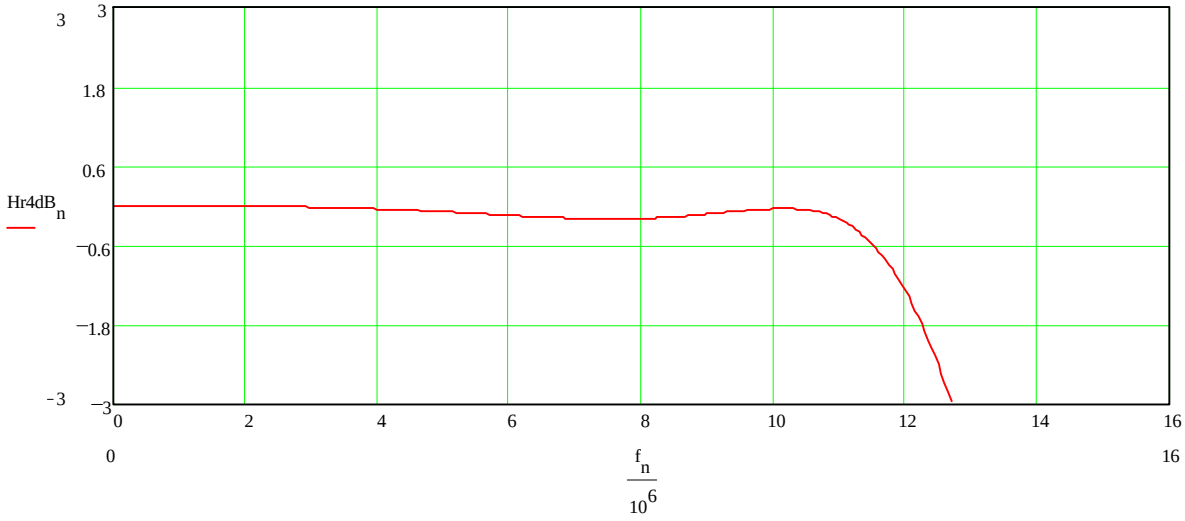

Figure 9: The detail of amplitude response of the pass band

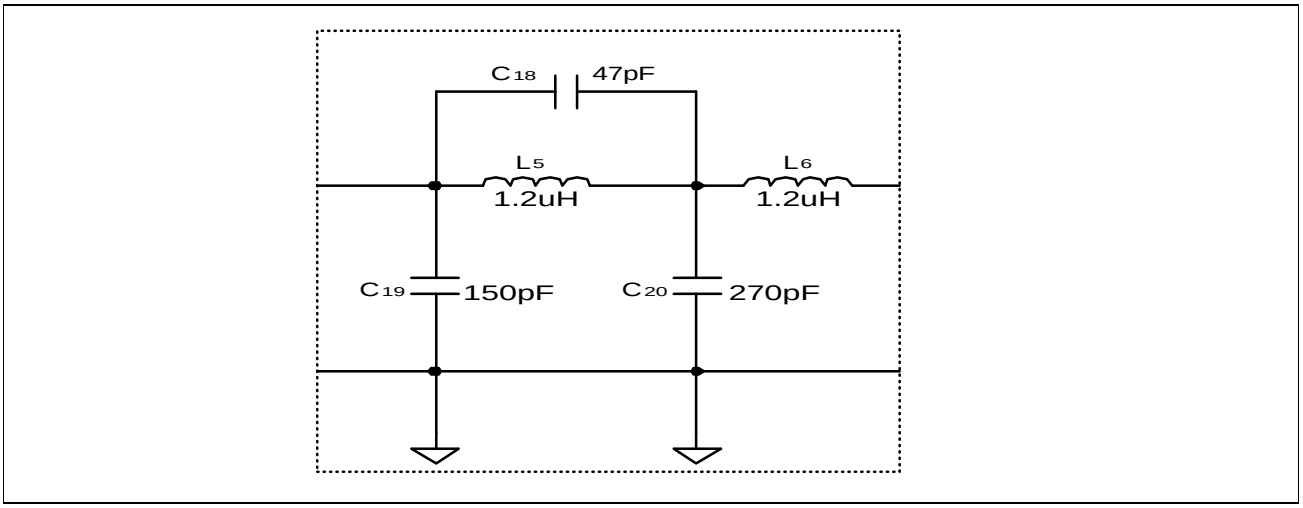

Figure 10 : Reconstruction filter diagram

The output of the CH7007/CH7008 may be configured for the following video output types: S-Video, composite, and SCART. **Figure 11** illustrates the typical connection for the S-Video and composite outputs, while **Figure 12** illustrates the connection for the SCART connector.

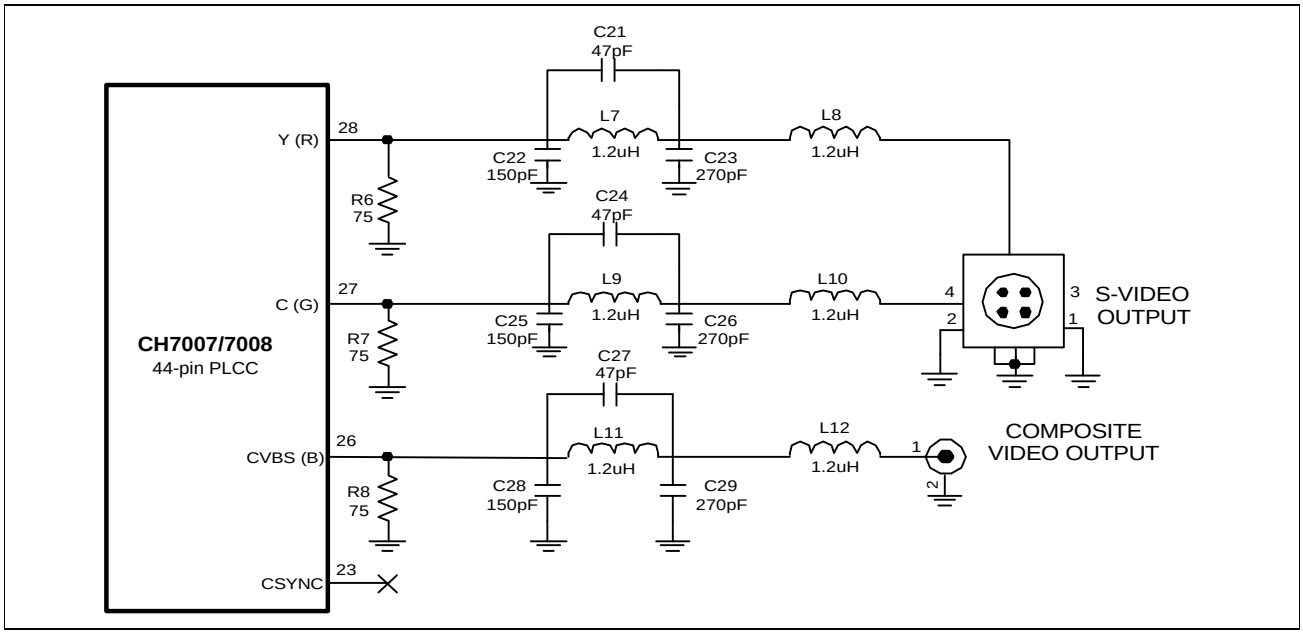

Figure 11: S-Video and Composite Video Outputs

Note: If the application only allows one video output connection and simultaneously display of S-Video and Composite is not needed, please refer AN27 on how to achieve the desire configuration.

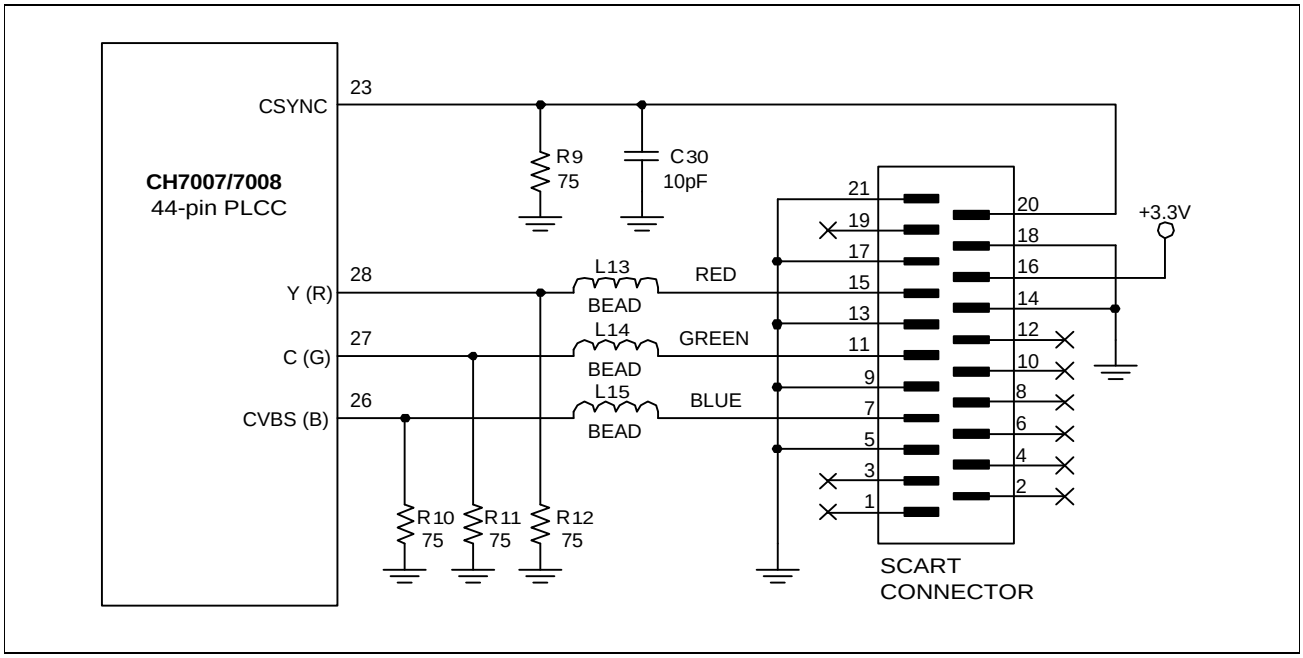

Figure 12: SCART Video Output

Careful layout consideration for the Y, C, CVBS traces and the attached components are needed in order to avoid the signal coupling among each other. It is suggested that the signal traces of Y, C and CVBS should be seperated with Ground traces and routed to the connectors. Also, the capacitors and the inductors attached to those outputs should not placed too close to each other.

Crystal Input

The 14.31818 MHz (±20ppm) crystal must be placed as close as possible to the XI/FIN and XO pins, with traces connected from point to point, overlaying the ground plane. Since the crystal generates timing reference for the CH7007/CH7008 encoders, it is very important that noise should not couple into these input pins. Traces with fast edge rates should not be routed under or adjacent these pins. In addition, the ground reference of the external capacitors connected to the crystal pins must be connected very close to the CH7007/CH7008.

Reference Crystal Oscillator

The CH7007/CH7008 includes an oscillator circuit which allows an inexpensive 14.31818 MHz crystal to be connected directly. Alternatively, an externally generated 14.31818 MHz clock source may be supplied to the CH7007/CH7008. If an external clock source is used, it should have CMOS level specifications. The clock should be connected to the XI/FIN pin, and the XO pin should be left open. The external source must exhibit ±20 ppm or better frequency tolerance, and possess low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

- Crystal is specified as 14.31818 MHz, ±20 ppm fundamental type and in parallel resonance (NOT series resonance).
- Crystal is operated with a load capacitance equal to its specified value (C_L).
- External load capacitors have their ground connection very close to the CH7007/CH7008 (C_{ext}).
- To allow tunability, a variable cap may be used from XI/FIN to ground

Note that the XI/FIN and XO pin each has approximately 10 pF (C_{int}) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI/FIN and XO pins, the following calculation should be used:

$$\mathbf{C_{ext} = (2 \times C_L) - C_{int} - 2C_S}$$

where:

- $\mathbf{C_{ext}}$ = external load capacitance required on XI/FIN and XO pins.
- $\mathbf{C_L}$ = crystal load capacitance specified by crystal manufacturer.
- $\mathbf{C_{int}}$ = capacitance internal to CH7007/CH7008 (approximately 10-15 pF on each of XI/FIN and XO pins).
- $\mathbf{C_S}$ = stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.)

Please refer to **Figure 13** for the symbols used in the calculation described above.

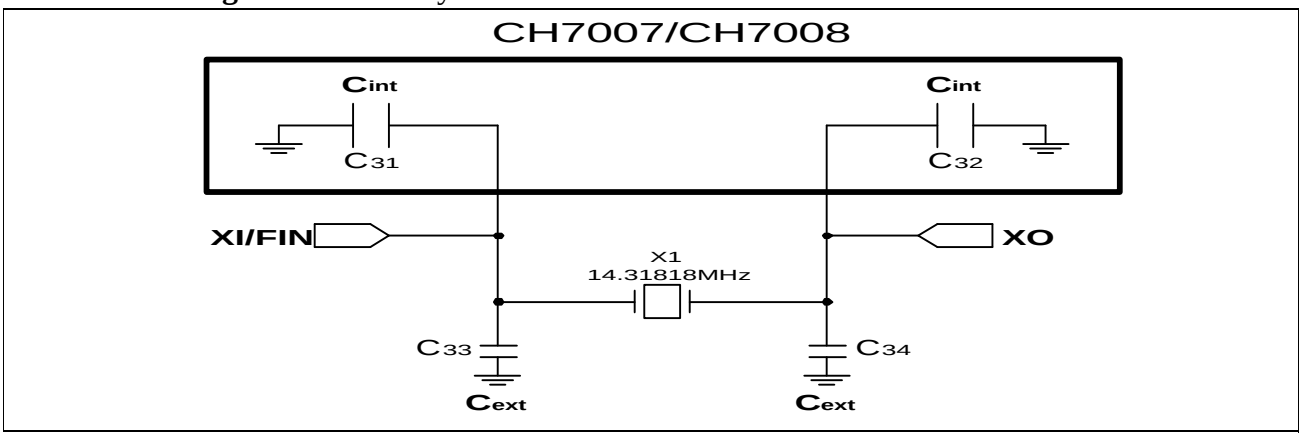

Figure 13: Reference Crystal

$$C_L = \frac{(C_{int\ XI/FIN} + C_{ext\ XI/FIN})\ (C_{int\ XO} + C_{ext\ XO})}{C_{int\ XI/FIN} + C_{int\ XO} + C_{ext\ XI/FIN} + C_{ext\ XO}} + C_S$$

In general , let us assume

$C_{int\ XI/FIN} = C_{int\ XO} = C_{int}$

$C_{ext\ XI/FIN} = C_{ext\ XO} = C_{ext}$

such that

$$C_L = \frac{C_{int} + C_{ext}}{2} + C_S \qquad \text{AND}$$

$C_{ext} = 2\ (C_L - C_S) - C_{int}$

$= 2\ C_L - (2C_S + C_{int})$

Therefore C_L must be specified greater than $C_{int}/2 + C_S$ in order to select C_{ext} properly.

Drive level

After C_L (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is not operating in excessive drive level specified by crystal manufacturer. Otherwrise, the crystal will age quickly and that in turn will affect the operating frequency of the cyrstal.

Drive level = 1/2 ($2\pi f \times C_L \times V$)^2 x R_S

R_S : Motion resistance is Ω. (≤ 50 Ω)

V: Operating voltage of crystal oscillator circuit.

f: Crystal operating frequency (14.31818 MH_Z).

For the detail consideration of crystal oscillator design, please refer AN-06.