PCB Layout and Design Considerations for CH7301 DVI Output Device

1. Introduction

This application note focuses on basic PCB layout and design guidelines for the CH7301 DVI Output Device. Guidelines in component placement, power supply decoupling, grounding, input signal interface and video components for DVI link implementation, are discussed in this document. The guidelines discussed here are intended to optimize the PCB layout and applications for this product. They are only for reference. Designers are urged to implement the configurations and evaluate the performance of the system prior to bringing the design to production.

The discussion and figures that follow reflect and describe connections based on the 64-pin LQFP package of CH7301. Please refer to CH7301 data sheet for the details of the pin assignments.

2. Component Placement and Design Considerations

Components associated with the CH7301 DVI transmitter should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1µF ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These capacitors (C7, C8, C9, C11, C12, C14, C15, C17) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7301 ground pins, in addition to ground vias.

2.1.1 Ground Pins

The analog and digital grounds of the CH7301 should connect to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7301 ground pins should connect directly to its respective decoupling capacitor ground lead, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. See **Table 1** for the Ground pins assignment.

2.1.2 Power Supply Pins

Separate digital (including the I/O supply voltage DVDDV), DVI, Analog, and DAC power planes are recommended. See **Table 1** for the Power supply pins assignment.

Table 1: Power Supply Pins Assignment in CH7301

Pin #	# of Pins	Type	Symbol	Description
1, 12, 49	3	Power	DVDD	**Digital Supply Voltage (3.3V)**
6, 11, 64	3	Power	DGND	**Digital Ground**
45	1	Power	DVDDV	**I/O Supply Voltage (1.1V to 3.3V)**
23, 29	2	Power	TVDD	**DVI Transmitter Supply Voltage (3.3V)**
20, 26, 32	3	Power	TGND	**DVI Transmitter Ground**
18,44	1	Power	AVDD	**PLL Supply Voltage (3.3V)**
16, 17, 41, 42	4	Power	AGND	**PLL Ground**
33	1	Power	VDD	**DAC Supply Voltage (3.3V)**
34, 40	2	Power	GND	**DAC Ground**

- **DVDDV & VREF Decoupling and Connection**

VREF is used as a reference level for pixel data input D[11:0], HSYNC input and VSYNC input. Please refer to **Figure 1** for optimum decoupling. In general applications, VREF is derived from DVDDV divided by 2, i.e., VREF = 1/2 x DVDDV.

Therefore, in **Figure 2**, both resistors should have the same value (10KΩ@ 1%). The decoupling capacitor is required as shown in **Figure 2**. Also, the DVDDV voltage supply should be connected to the graphics controller I/O supply voltage.

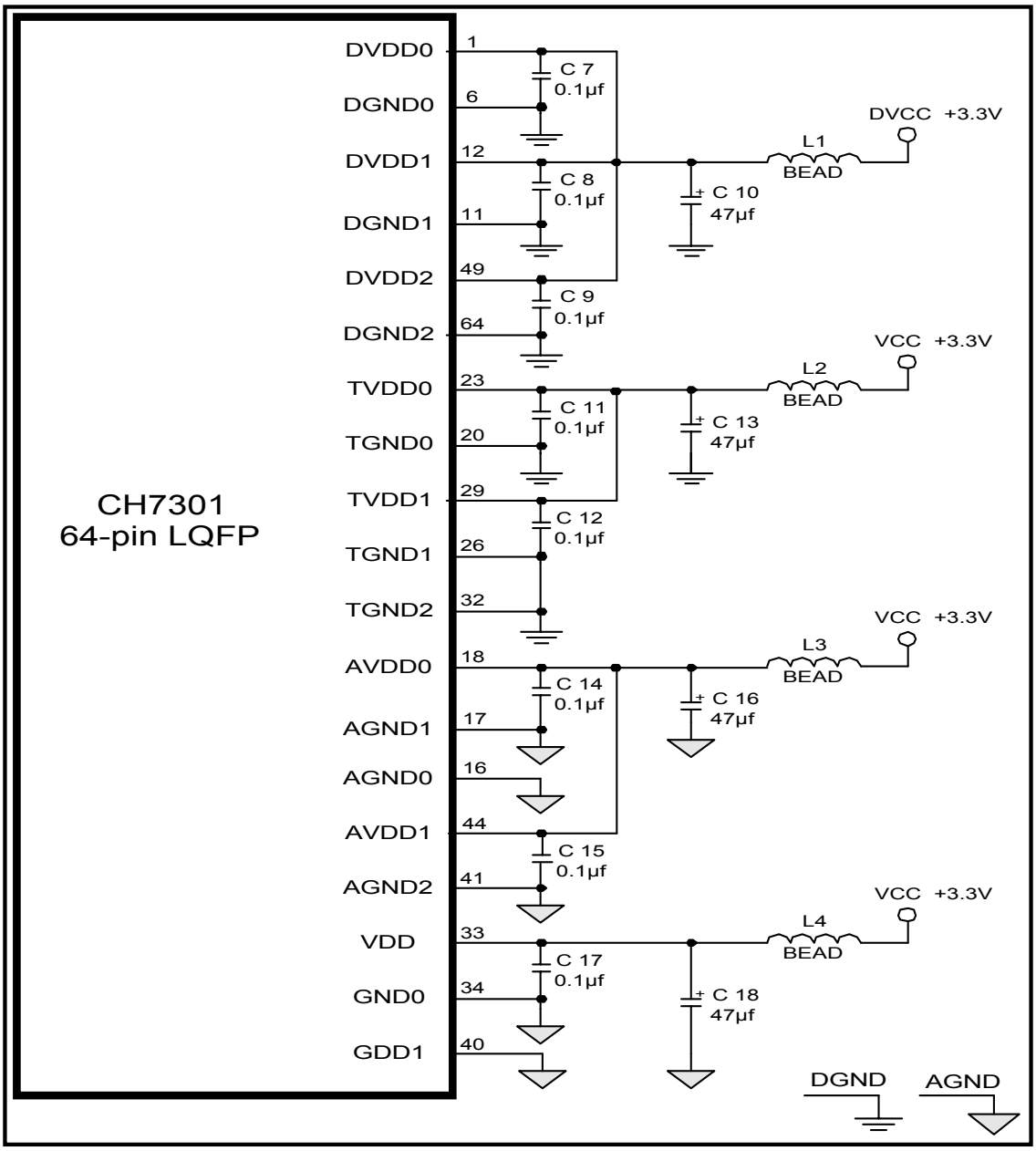


Figure 1: Power Supply Decoupling and Distribution

Notes: All the Ferrite Beads described in this document are recommended to have an impedance of less then 0.05Ω at DC; 23Ω at 25MHz & 47Ω at 100MHz. Please refer to Fair_Rite part# 2743019447 for details or an equivalent part can be used for the diagram.

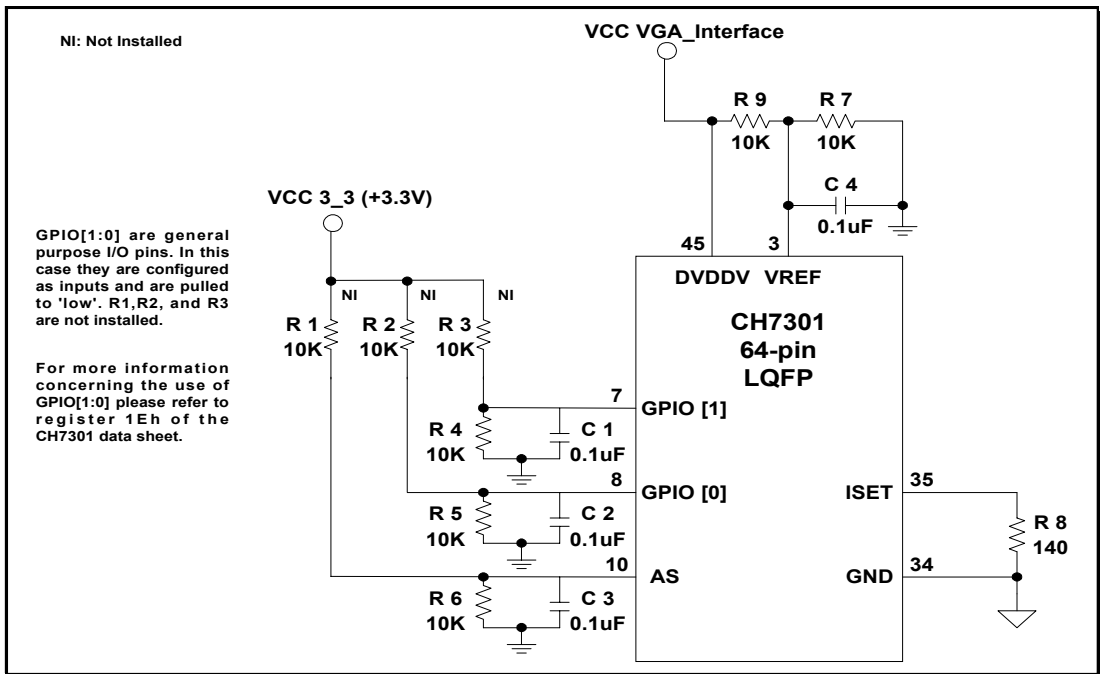


Figure 2: ISET, VREF, DVDDV, GPIO and AS connection

- ## TVDD Power Connection

One of the two recommended TVDD power connections shown in **Figure 3** and **Figure 4**, should be implemented to avoid power back-drive problems as described in AN57. TVDD Power Connection 2, **Figure 4**, is preferred so that TVDD can be well regulated at 3.3V. Please refer to AN57 for more details.

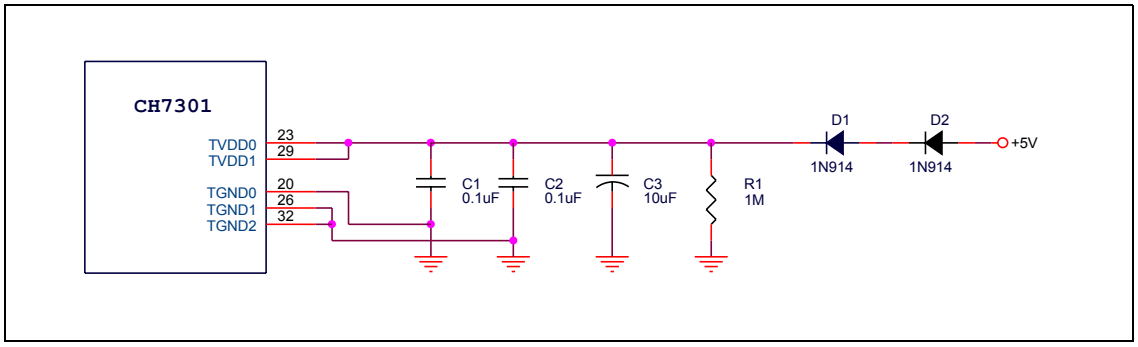


Figure 3: TVDD Power Connection 1

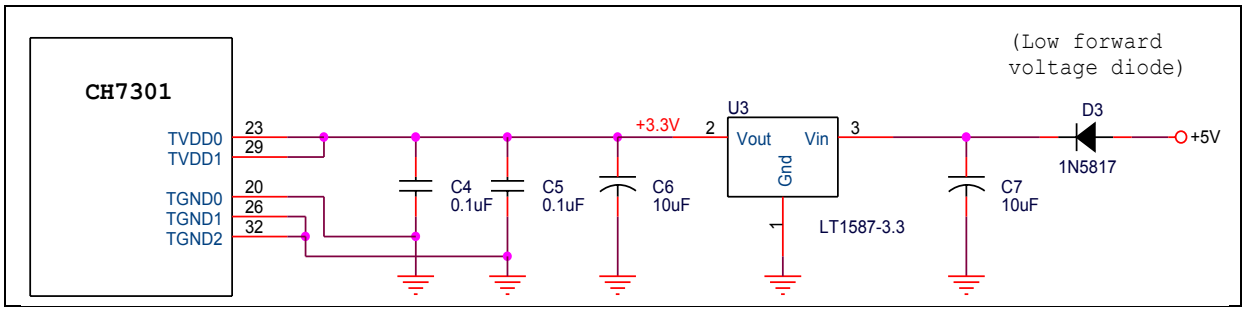


Figure 4: TVDD Power Connection 2

2.2 General Control

- **ISET pin**

The ISET pin, pin 35, sets the DAC current. A 130Ω – 140Ω resistor should be placed as close as possible to the ISET pin using short and wide traces. Whenever possible, the ISET resistor ground pin should also be connected to pin 34. Otherwise, the ground reference of the ISET resistor should ideally be close to the CH7301. See **Figure 2** for design reference.

With a 140Ω resistor connected to the ISET pin, the peak white level and color saturation will be slightly lower than the standard. However, the DACs will consume less current. Alternatively, with a 130Ω resistor connected to the ISET pin, the peak white level will be higher and color will be more saturated, however, the DACs will consume more current.

- **Data Enable pin**

The Data Enable pin, pin 2, is an input pin and accepts the Data Enable signal from the VGA graphics chipset. Active video data is indicated when the VGA drives the Data Enable signal 'high'. When the Data Enable signal is 'low', the video data will not be encoded and driven out of the DVI interface. The voltage levels are between 0V and DVDDV, and the VREF signal is used as the threshold level.

- **GPIO [0] & GPIO[1] pins**

GPIO[1:0] are General Purpose I/O pins. To set the direction of these pins, register 1Eh, the GPIO Control Register must be set accordingly. The GPIO[1] pin can be configured as an output for the DVI link detect signal. In this configuration, this pin will be driven low when a termination change has been detected on the HPDET input.

- **AS pin**

The Address Select pin, pin 10, can be configured as shown in **Figure 2**. This pin determines the serial port address of the device. If AS is pulled 'low', then the serial port address is 0x76h, if AS is pulled 'high', then the serial port address is 0x75h.

Note: To use the Intel driver for the CH7301, the AS pin must be pulled 'low'.

- **Video Inputs (D[0:11])**

Since the digital pixel data and the pixel clock of the CH7301 may toggle at speeds up to165MHz (depending on the input mode), it is critical that the connection of these video signals between the graphics controller and the CH7301 be kept short and isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals. The DATA signals are single ended high speed signals that should be routed together as a bus. It is recommended that 8 mil traces be used in routing these signals.

- **Buffered Clock Output (BCO)**

The clock output from the BCO/VSYNC pin, pin 47, is controlled by register 22h, the BCO (Buffered Clock Output) register. Bits 2-0 select the signal output (see **Table 2**). The VGA vertical sync is the only clock output available to output in the current version. The BCO/VSYNC pin should be connected to the VS pin of DVI-I connector if VGA bypass is to be implemented. If VGA bypass is not implemented then the BCO/VSYNC pin can be left floating.

Table 2: BCO Output Signal

BCO[2:0]	Buffered Clock Output	BCO[2:0]	Buffered Clock Output
000	Not Valid	100	Not Valid
001	Not Valid	101	Not Valid
010	Not Valid	110	VGA Vertical Sync
011	Not Valid	111	Not Valid

2.3 Serial Port Interface

- **SPD and SPC pins**

  SPD (pin 14) and SPC (pin 15) function as a serial interface where SPD is bi-directional data and SPC is an input only serial clock. In the reference design, SPD and SPC are pulled up with 1 KΩ resistors.

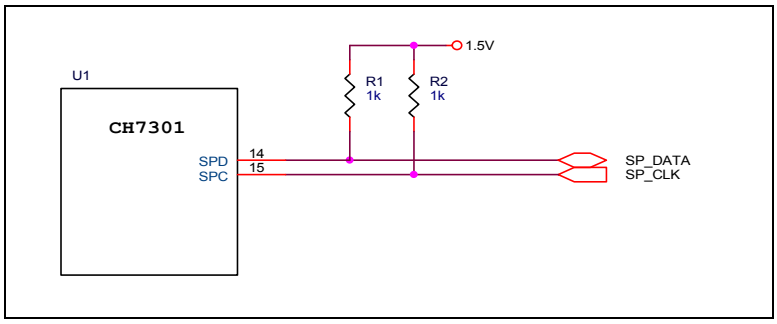


Figure 5: Serial Port Interface

2.4 DVI Output and Control

In DVI output mode, the multiplexed input data, sync and clock signals are input to the CH7301 from the graphics controller's digital output port. Data will be 2X multiplexed, and the clock inputs can be 1X or 2X times the pixel rate. For correct DVI operation, the input data format must be selected to be one of the RGB input formats.

The TDC0, TDC1, TDC2 & TLC signals are high frequency differential signals that need to be routed with special precautions. Since the TDC0, TDC1, TDC2 & TLC signals are differential they must be routed in pairs: TDC0 & TDC0*, TDC1 & TDC1*, TDC2 & TDC2*, TLC & TLC* signals. The lengths of the 4 pair of signals must be kept as close to the same as possible. The maximum length difference must not exceed 100 mils for any of the pairs relative to each other. The number of bends should be kept to 4 or less and 45 degree is the maximum corner angle. These signals should be routed on the top layer directly to the DVI connector without any vias to the bottom layer. The pin placement of the TDC0, TDC1, TDC2 & TLC signals allows for a direct route to the DVI connector. The CH7301 comes in versions able to drive a DVI display at a pixel rate of up to 165 MHz, supporting UXGA resolution displays. No scaling of input data is performed on the data output to the DVI device.

Figure 6 shows an example of the connection of the DVI output. In the figure a DVI-I Right Angle Connector is used to interface the CH7301 DVI outputs to the monitor.

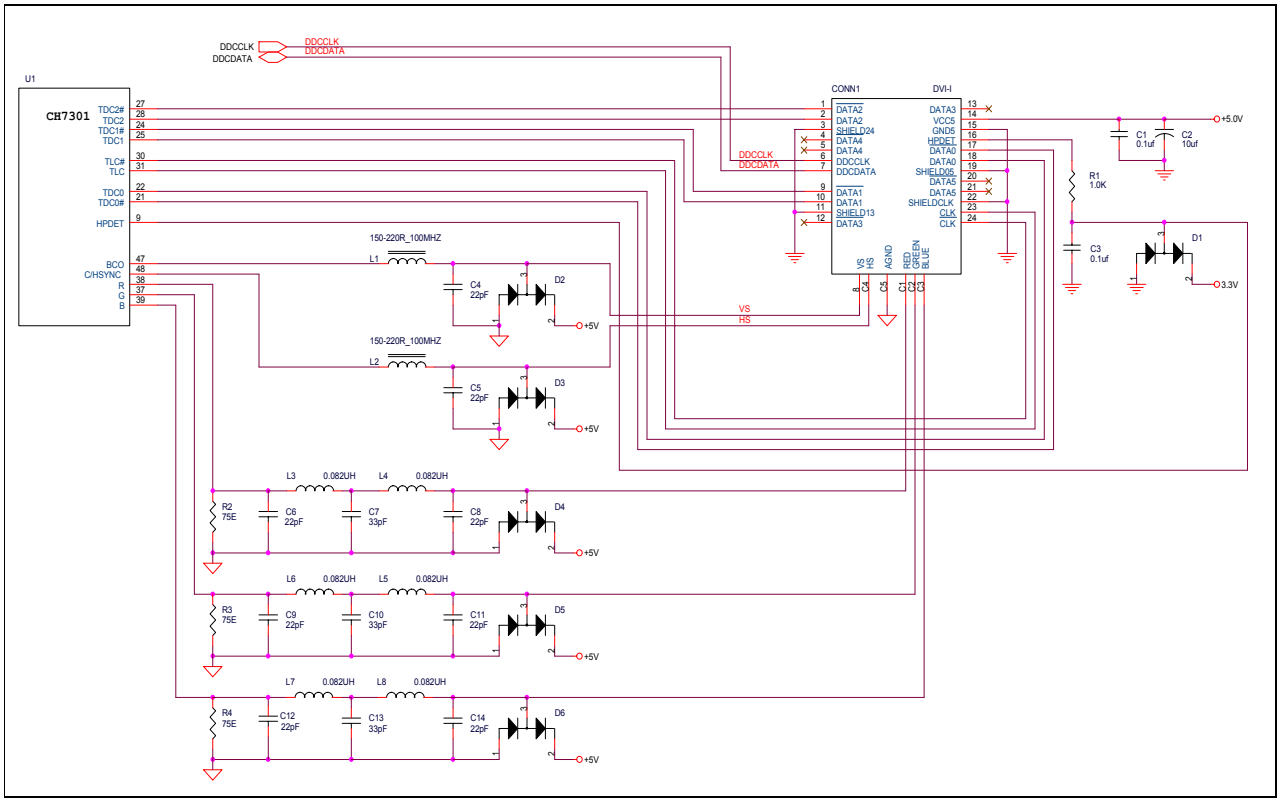


Figure 6: DVI-I Output Connection

- **DVI Link Detect Output (TLDET*) (internal pull-up)**

  The CH7301 comes in versions able to drive a DVI display at a pixel rate of up to 165 MHz, supporting UXGA resolution displays. No scaling of input data is performed on the data output to the DVI device.

  The TLDET* pins (Pins 7 and Pin 46) provides a general purpose I/O controlled via the serial port interface. No internal pull-up when TLDET* is selected. When the GPIO[1]/TLDET* pin is configured as an output, this pin can be used to output the DVI link detect signal (pulls low when a termination change has been detected on the HPDET input). This is an open drain output. The output is released through serial port interface (See **Figure 6**). Also there are two different pins within the CH7301 (pin 7 or pin 46) can be used to feed back to the graphics device when there has been a change in the state of the hot plug detect (HPDET) pin. Pin 7 is enabled when GOENB[1] is set high, and HPIE2 is set high. Pin 46 is enabled when POUTE is low, and HPIE is high. Whichever pin is enabled for the TLDET* function will pull low with an open drain output following a transition on the HPDET input.

- **DVI Data Channel (TDC[0:2] and TDC[0:2]*)**

  These pins (Pins 22, 25, 28 for TDC[0:2] and Pins 21, 24, 27 for TDC[0:2]*) provide the DVI differential outputs for data channel 0 (blue), channel 1(green) and channel 2 (red) (See **Figure 6**).

- **DVI Link Clock Outputs (TLC and TLC*)**

  These pins (Pins 30, 31) provide the DVI differential clock outputs for the DVI interface corresponding to data on the TDC[0:2] outputs (See **Figure 6**).

- **HPDET (DVI Hot Plug Detect)**

  This input pin (Pin 9) determines whether the DVI link is connected to a DVI monitor. When terminated, the monitor is required to apply a voltage greater than 2.4 volts. Changes on the status of this pin will be relayed to the graphics controller via the TLDET* or GPIO[1]/TLDET* pin pulling low (See **Figure 6**).

- **VSWING (DVI Link Swing Control)**

  This pin (Pin 19) sets the swing level of the DVI outputs. A 2.4KΩ resistor should be connected between this pin and GND using short and wide traces.

2.5 Analog RGB Output

The R, G, B (pins 38, 37, 39) signals are analog video signals. These signals should be routed using 75Ω traces. These signals should not be routed together. There should be a minimum of 12 mils spacing between each of the R, G, B signals and 20 mils spacing between them and any digital trace.

Typically these signals should be routed in a separate analog area without any digital signal running through the area. Corners for these traces should be at a maximum of 45 degree. 90 degree corner should not be used due to cross coupling between adjacent traces. These traces should be kept on the top layer to minimize the use of vias on them.

In **Figure 6**, the input protection diodes D1 - D6 should be placed as close to the DVI connector as possible and the series termination resistors R2-R4 should be placed as close to the CH7301 as possible. If the analog outputs of the DVI-I connector are to be used, the ferrite beads L1-L8 should be placed as close to the DVI-I connector as possible to reduce EMI emissions.

2.6 PCB Design Considerations for Migrating from CH7301 to CH7303

The CH7303 DVI transmitter is an enhanced version of the CH7301 DVI transmitter with HDTV output. In addition, the CH7303 has 16 pins of data input channel and the CH7301 has 12 pins of data inputs. **Figure 7** shows the recommended CH7301 PCB design which accommodates the CH7303. If the PCB designer intends to migrate from the CH7301 to the CH7303 in the future, the only thing that has to be concerned is pulling down all the unused data input pins, D[15:12], of the CH7303. For more details on the CH7303, please refer to the CH7303 data sheet.

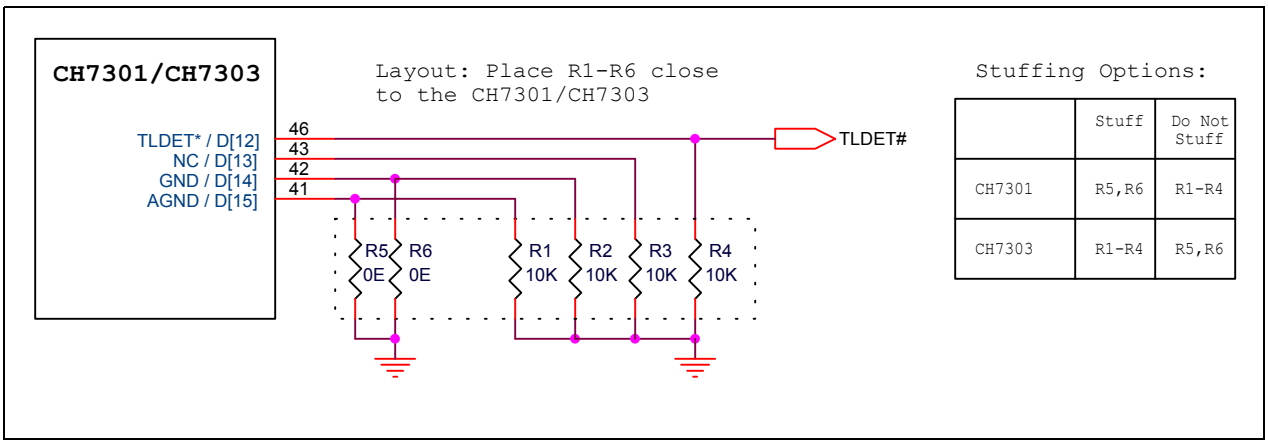
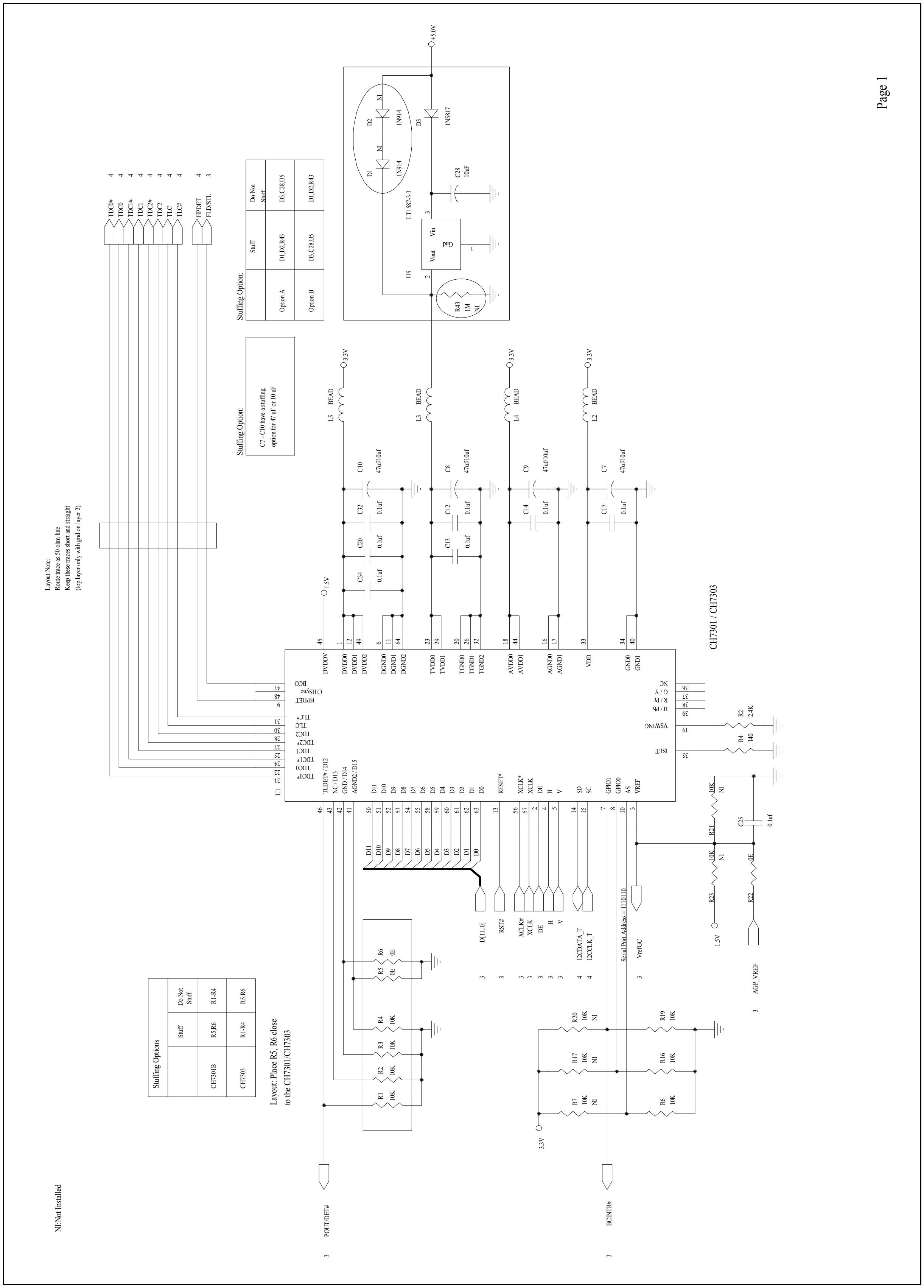


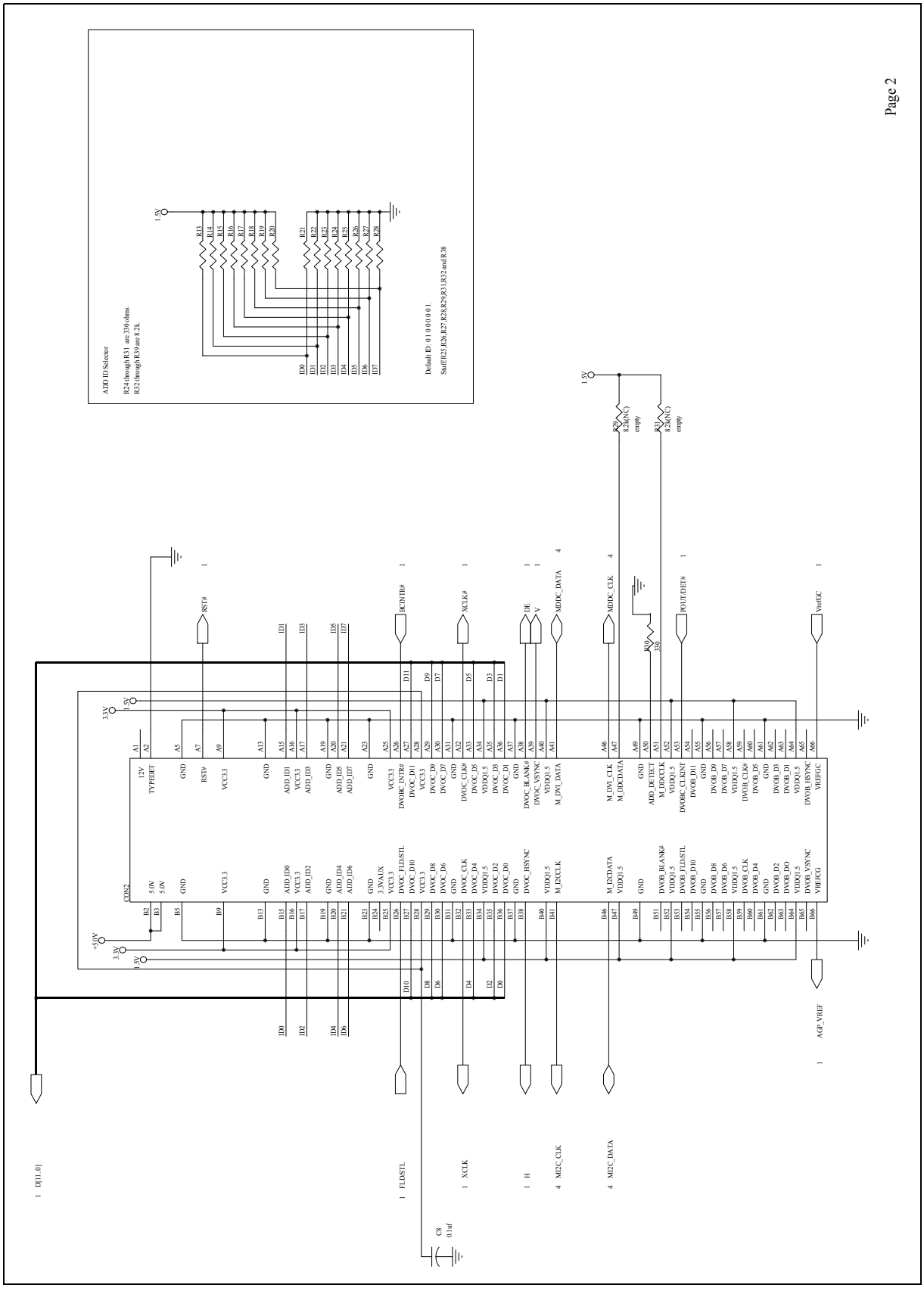
Figure 7: CH7303 PCB Implementation for an Existing CH7301 PCB Design

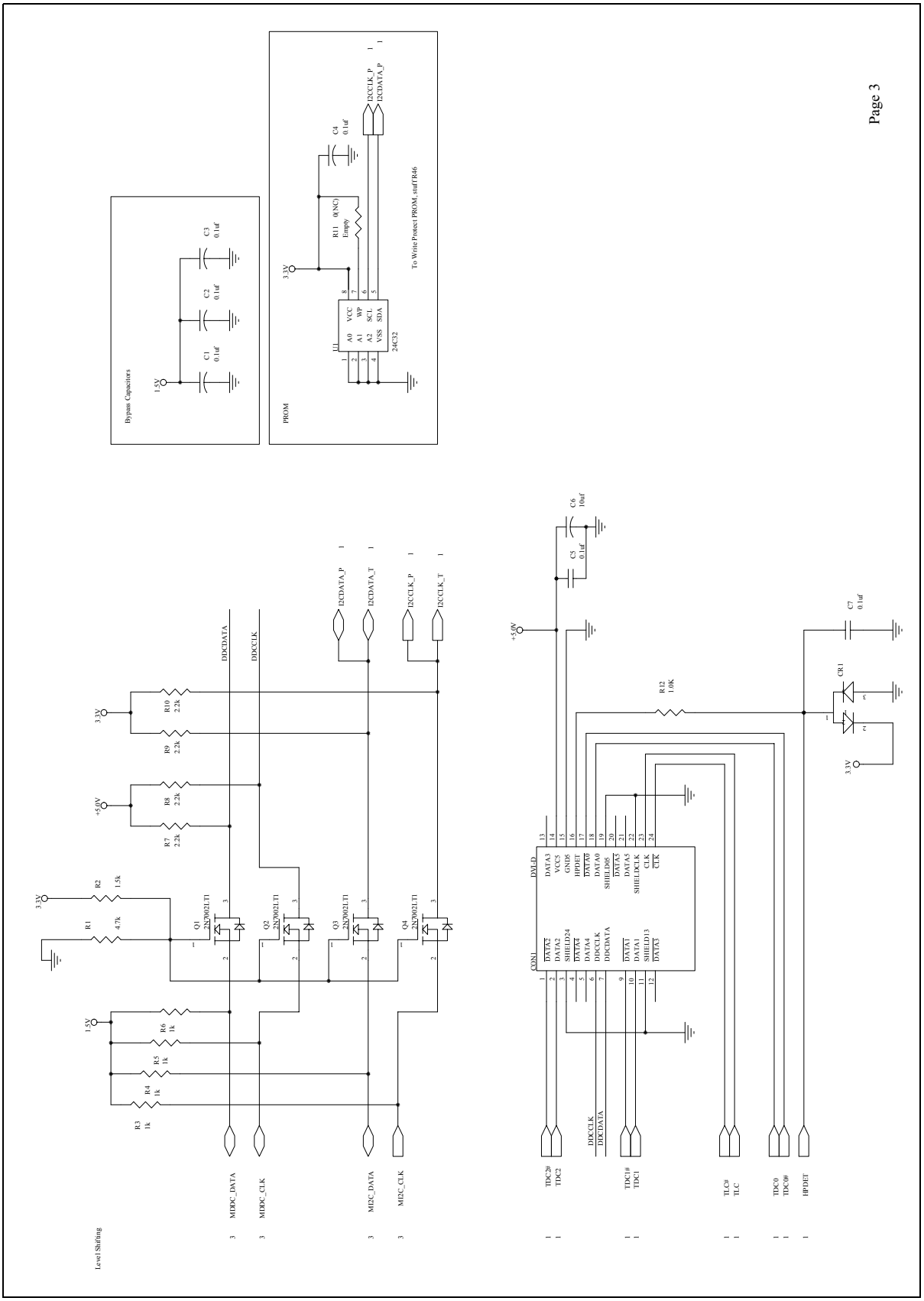
3. Reference Design Example

The following schematics are based on an Intel Brookdale® / Montara® / Springdale® Graphics chipset design and are to be used as a CH7301 PCB design example only. It is not a complete design. Those who are seriously doing an application design with CH7301 and would like to have a complete reference design schematic, should contact Applications within Chrontel, Inc.

3.1 Schematics of Reference Design Example


CH7301 / CH7303
Page 1
NI:Not Installed
Layout Note:
Route trace as 50 ohm line
Keep these traces short and straight
(top layer only with gnd on layer 2).
Stuffing Option:
C7 - C10 have a stuffing
option for 47 uF or 10 uF
Stuffing Option:
Option A
Option B
Stuff
Do Not Stuff
D1,D2,R43
D3,C28,U5
Stuffing Options
CH7301B
CH7303
R5,R6
R1-R4
Layout: Place R5, R6 close
to the CH7301/CH7303
LT1587-3.3
+5.0V
3.3V
1.5V
BEAD
POUTDET#
BCINTR#
AGP_VREF
Serial Port Address = 1110110
VrefGC
D[11..0]
RST#
XCLK#
XCLK
DE
H
V
I2CDATA_T
I2CCLK_T
HPDET
FLD/STL


Page 2
ADD ID Selector
R24 through R31 are 330 ohms.
R32 through R39 are 8.2k.
Default ID: 0 1 0 0 0 0 0 1.
Set R25, R26, R27, R28, R29, R31, R32 and R38
1.5V
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
ID0
ID1
ID2
ID3
ID4
ID5
ID6
ID7
CON2
12V
TYPEDET
5.0V
GND
RST#
VCC3.3
ADD_ID1
ADD_ID3
ADD_ID5
ADD_ID7
DVOBC_INTR#
DVOC_D11
DVOC_D9
DVOC_D7
DVOC_CLK#
DVOC_D5
DVOC_D3
DVOC_D1
DVOC_BLANK#
DVOC_VSYNC
M_DVI_DATA
M_DVI_CLK
M_DDCDATA
ADD_DETECT
M_DDCCLK
DVOBC_CLKINT
DVOB_D11
DVOB_D9
DVOB_D7
DVOB_CLK#
DVOB_D5
DVOB_D3
DVOB_D1
DVOB_VSYNC
VREFGC
3.3VA/UX
DVOC_FLDSTL
DVOC_D10
DVOC_D8
DVOC_D6
DVOC_CLK
DVOC_D4
DVOC_D2
DVOC_D0
DVOC_HSYNC
M_I2CDATA
M_I2CCLK
DVOB_BLANK#
DVOB_FLDSTL
DVOB_D10
DVOB_D8
DVOB_D6
DVOB_CLK
DVOB_D4
DVOB_D2
DVOB_D0
DVOB_HSYNC
VREFDG
+5.0V
3.3V
1.5V
3.3V
1.5V
R29
8.2k(NC)
empty
R30
8.2k(NC)
empty
R31
330
MDDC_CLK
MDDC_DATA
RST#
DCINTR#
XCLK#
DE
V
POUT/DET#
VrefGC
AGP_VREF
1 D[11..0]
1 FLDSTL
1 XCLK
1 H
4 MI2C_CLK
4 MI2C_DATA
C8
0.1uf


Page 3
Bypass Capacitors
C1 0.1uf
C2 0.1uf
C3 0.1uf
1.5V
PROM
U1
24C32
R11 (0 NC) Empty
C4 0.1uf
To Write Protect PROM, stuff R46
I2CCLK_P
I2CDATA_P
DDCDATA
DDCCLK
R10 2.2k
R9 2.2k
R8 2.2k
R7 2.2k
R1 4.7k
R2 1.5k
R3 1k
R4 1k
R5 1k
R6 1k
Q1 2N3902LT1
Q2 2N3902LT1
Q3 2N3902LT1
Q4 2N3902LT1
I2CDATA_T
I2CCLK_T
MDDC_DATA
MDDC_CLK
MI2C_DATA
MI2C_CLK
Level Shifting
C5 0.1uf
C6 10uf
C7 0.1uf
R12 1.0K
CR1
CON1
DVI-D
DATA3
VCC5
GND6
HPDET
DATA0
DATA0
SHIELD6
DATA5
DATA5
SHIELDCLK
CLK
CLK
DATA2
DATA2
SHIELD24
DATA4
DATA4
DDCCLK
DDCDATA
DATA1
DATA1
SHIELD13
DATA3
TDC2#
TDC2
TDC1#
TDC1
TLC#
TLC
TDC0
TDC0#
HPDET

4. Revision History

Revision	Date	Section	Description
1.0	6/16/00	All	First official release, revision 1.0
2.0	1/30/03	All	All Figures and Tables updated.
		2.1.2	ISET resistor value description added.
		2.6	CH7301 to CH7303 PCB migration implementation added.
		3.0	Reference schematics changed to a Intel Bookdale® / Montara® / Springdale® reference design.

Disclaimer

This document provides technical information for the user. Chrontel reserves the right to make changes at any time without notice to improve and supply the best possible product and is not responsible and does not assume any liability for misapplication or use outside the limits specified in this document. We provide no warranty for the use of our products and assume no liability for errors contained in this document. The customer should make sure that they have the most recent data sheet version. Customers should take appropriate action to ensure their use of the products does not infringe upon any patents. Chrontel, Inc. respects valid patent rights of third parties and does not infringe upon or assist others to infringe upon such rights.

Chrontel PRODUCTS ARE NOT AUTHORIZED FOR AND SHOULD NOT BE USED WITHIN LIFE SUPPORT SYSTEMS OR NUCLEAR FACILITY APPLICATIONS WITHOUT THE SPECIFIC WRITTEN CONSENT OF Chrontel. Life support systems are those intended to support or sustain life and whose failure to perform when used as directed can reasonably expect to result in personal injury or death.

Chrontel

2210 O'Toole Avenue, Suite 100,
San Jose, CA 95131-1326
Tel: (408) 383-9328
Fax: (408) 383-9338
www.chrontel.com
E-mail: sales@chrontel.com