PCB Layout and Design Considerations for CH7011 TV Output Device

1. Introduction

This application note focuses on the basic PCB layout and design guidelines for the CH7011 TV Output Device. Guidelines in component placement, power supply decoupling, grounding, and reference crystal placement and selection, input signal interface and video components for the TV output are discussed in this document. The guidelines discussed here are intended to optimize the PCB layout and applications for this product. They are only for reference. Designers are urged to implement the configurations and evaluate the performance of the system prior to bringing the design to production.

The discussion and figures that follow reflect and describe connections based on the 64-pin LQFP package of the CH7011.

2. Component Placement and Design Considerations

Components associated with the CH7011 TV transmitter should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1µF ceramic capacitor to each of the power supply pins as shown in **Figure 1** and **Figure 2**. These capacitors (C7, C8, C9, C14, C15, C17) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7011 ground pins, in addition to ground vias.

2.1.1 Ground Pins

The analog and digital grounds of the CH7011 should connect to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7011 ground pins should connect directly to its respective decoupling capacitor ground lead, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. See **Table 1** for the Ground pins assignment.

2.1.2 Power Supply Pins

Separate digital (including the I/O supply voltage DVDDV), Analog, and DAC power planes are recommended. See **Table 1** for the Power supply pins assignment.

Table 1: Power Supply Pins Assignment in CH7011

Pin Assignment	# of Pins	Type	Symbol	Description
1, 12, 49	3	Power	DVDD	**Digital Supply Voltage (3.3V)**
6, 11, 64	3	Power	DGND	**Digital Ground**
45	1	Power	DVDDV	**I/O Supply Voltage (1.1V to 3.3V)**
18, 44	2	Power	AVDD	**PLL Supply Voltage (3.3V)**
16, 17, 41	3	Power	AGND	**PLL Ground**
33	1	Power	VDD	**DAC Supply Voltage (3.3V)**
34, 40	2	Power	GND	**DAC Ground**

- **DVDDV & VREF Decoupling and Connection**

VREF is used as a reference level for pixel data input D[11:0], HSYNC input, VSYNC input, P-OUT output. Please refer to **Figure 1** for optimum decoupling. In general applications, VREF is derived from DVDDV divided by 2, i.e., VREF = 1/2 × DVDDV.

Therefore, in **Figure 2**, both resistors should have the same value (10KΩ @ 1%). The decoupling capacitor, C4, is required as shown in **Figure 2**. Also the DVDDV voltage supply should be connected to the graphics controller I/O VDD.

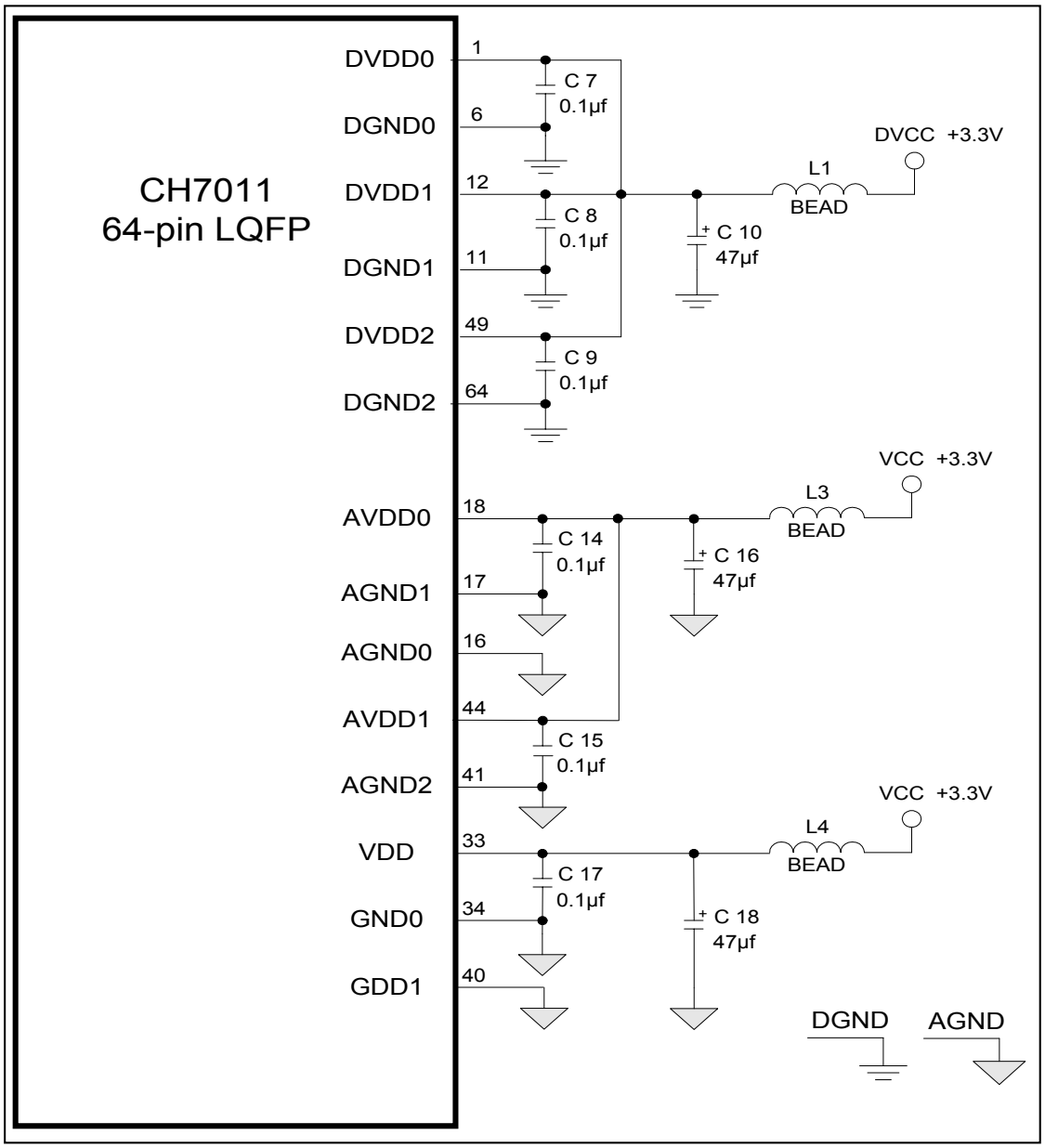


Figure 1: Power Supply Decoupling and Distribution

Notes: All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05Ω at DC; 23Ω at 25MHz & 47Ω at 100MHz. Please refer to Fair_Rite part# 2743019447 for details or an equivalent part can be used for the diagram.

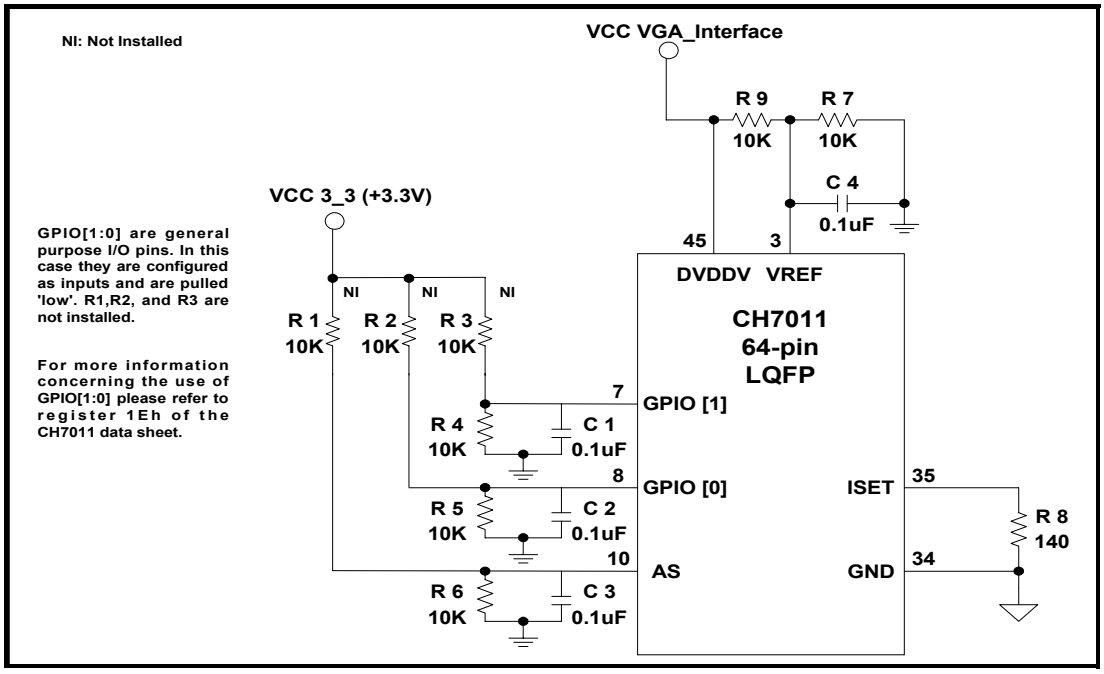


Figure 2: (1) ISET, VREF and DVDDV Connection; (2) GPIO and AS connection

2.2 General Control and Inputs

- **ISET pin**

The ISET pin, pin 35, sets the DAC current. A 130Ω – 140Ω resistor should be placed as close as possible to the ISET pin using short and wide traces. Whenever possible, the ISET resistor ground pin should also be connected to pin 34. Otherwise, the ground reference of the ISET resistor should ideally be close to the CH7011. See **Figure 2** for design reference.

With a 140Ω resistor connected to the ISET pin, the peak white level and color saturation will be slightly lower than the standard. However, the DACs will consume less current. Alternatively, with a 130Ω resistor connected to the ISET pin, the peak white level will be higher and color will be more saturated, however, the DACs will consume more current.

- **GPIO [0] & GPIO[1] pins**

GPIO[1:0] are General Purpose I/O pins. To set the direction of these pins, register 1Eh, the GPIO Control Register must be set accordingly.

In applications using the Intel Brookdale®, Montara®, or Springdale® chipset and software driver, it is recommended that GPIO[1:0] be layed out as shown in **Figure 2**. The Intel software driver uses GPIO[0] to select the TV output mode. For NTSC, the GPIO[0] pin must be pulled 'low' and for PAL, the GPIO[0] pin must be strapped 'high'. As for the GPIO[1] pin, the current Intel software driver only implements the state in which GPIO[1] is pulled 'high'. When GPIO[1] is 'high', TV video is outputted to the corresponding DAC pins.

- **AS pin**

The Address Select pin, pin 10, can be configured as shown in **Figure 2**. This pin determines the serial port address of the device. If AS is pulled 'low', then the serial port address is 0x76h, if AS is pulled 'high', then the serial port address is 0x75h.

Note: To use the Intel driver for the CH7011, the AS pin must be pulled 'low'.

- **Horizontal and Vertical Sync Signals (HSYNC and VSYNC)**

  In input modes where the horizontal and vertical sync signals from the graphics controller are shared between the CH7011 and the computer monitor, buffering the sync signals prior to connecting them to the monitor is recommended (please refer to **Figure 3**). These buffers help isolate any noise generated from the monitor connection (e.g., reflections, etc.) from coupling into the sync inputs of the CH7011, thereby degrading the display quality. In modes where the embedded syncs are used, these buffers are not necessary.

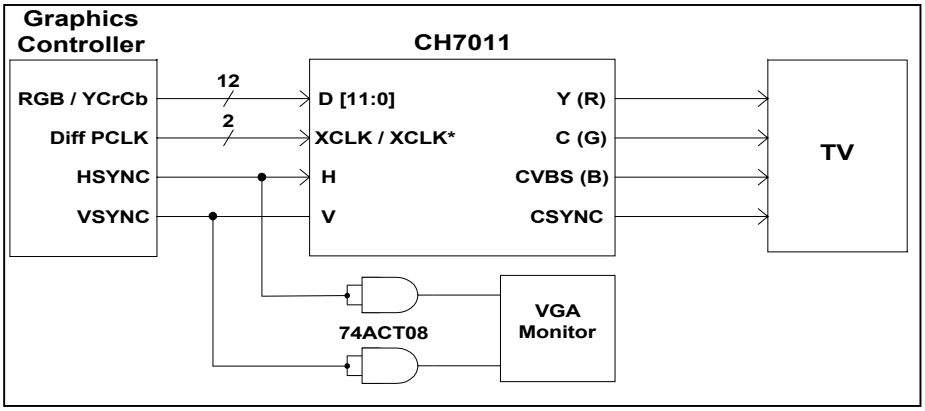


Figure 3: Sync Buffers

Note: If differential pixel clock from the graphics controller is not available, XCLK* should be tied to VREF.

- **Video Inputs (D[0:11])**

  Since the digital pixel data and the pixel clock of the CH7011 may toggle at speeds of up to 165MHz (depending on input mode), it is critical that the connection of these video signals between the graphics controller and the CH7011 be kept short and isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals. The DATA signals are single ended high speed signals that should be routed together as a bus. It is recommended that 8 mil traces be used in routing these signals.

- **Pixel Clock Mode**

  Depending on the architecture and configuration of the graphics controller, CH7011 may have different clock modes settings. In all these modes, HSYNC, VSYNC and pixel data D[11:0] must meet the setup and hold time with respect to pixel clock.

- **Master Clock Mode**

  When the CH7011 is operating in TV Out mode, the P-OUT/TLDET pin outputs a pixel clock to the graphics controller. To enable Master Clock Mode for the CH7011, bit 3 of the CM register, reg. 1Ch, should set to 1. The 14.31818MHz clock is then used as a frequency reference in the TV PLL. Bit 0 of the CM register signifies the XCLK frequency. A value of 0 should be written to the CM register when the XCLK is at the pixel frequency (duel edge clocking mode) and a value of 1 is used when the XCLK is twice the pixel frequency (single edge clocking mode).

  Bit 1 of the CM Register controls the P-OUT clock frequency. A value of 0 generates a clock output at the pixel frequency, while a value of 1 generates a clock at twice the pixel frequency.

  Bit 2 of the CM register controls the phase of the XCLK clock input to the CH7011. A value of 1 inverts the XCLK signal at the input of the device. This control is used to select which edge of the XCLK signal to use for latching the input data.

The direction of HSYNC and VSYNC signal can be controlled by the Sync Register, reg. 1Fh. When bit 5, the SYO bit, = 0, the HSYNC and VSYNC signals are input to CH7011. When the bit 5 = 1, the HSYNC and VSYNC signals are output to graphics controller. It is recommended to configure CH7011 in this clock mode with SYO set to 0 when the application use with the Intel Brookdale or Intel Springdale (See **Figure 4** for design details).

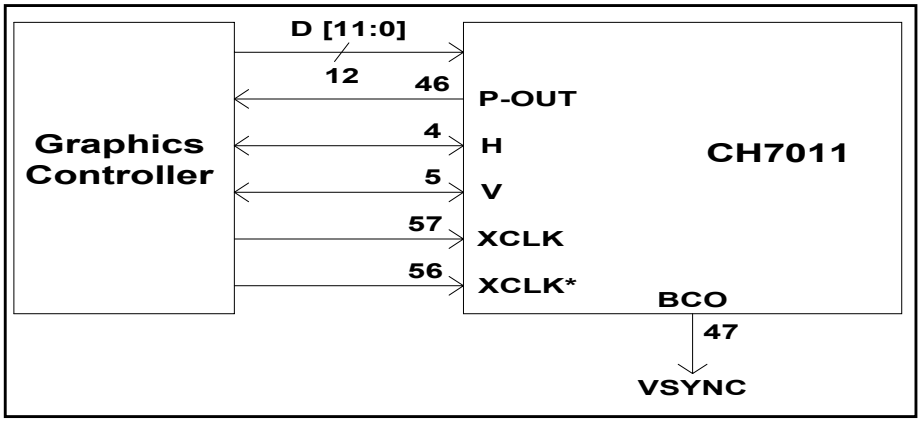


Figure 4: Master Clock Mode

- **BCO pin**

When BCO is used to provide a Buffered Clock Output, the output clock can be selected using the BCO Register (reg. 22h). **Table 2** shows the details of the buffered output clock modes.

Table 2: BCO Output Signal

BCO[2:0]	Buffered Clock Output	BCO[2:0]	Buffered Clock Output
000	The 14MHz crystal	100	Sine ROM MSB
001	UCLK	101	Cosine ROM MSB
010	VCO divided by K3	110	VGA Vertical Sync
011	Field ID	111	TV Vertical Sync

- **Slave Clock Mode**

For this mode, register 1Ch (Clock Mode Register, CM) bit 3 must be set to 0. The pixel clock comes from the graphics controller and the P-OUT pin is in a high impedance state (not automatically). The XCLK input is then used as a reference to the TV PLL. The direction of the HSYNC and VSYNC signals can be controlled by the Sync Register, reg. 1Fh. When bit 5 of the SYO register = 0, the HSYNC and VSYNC signals are input to CH7011. When bit 5 of the SYO register = 1, the HSYNC and VSYNC signals are output to graphics controller. It is recommended to configure CH7011 in this clock mode with SYO set to 0 when the application uses the Intel Brookdale or Intel Springdale chipsets (See **Figure 5** for design details).

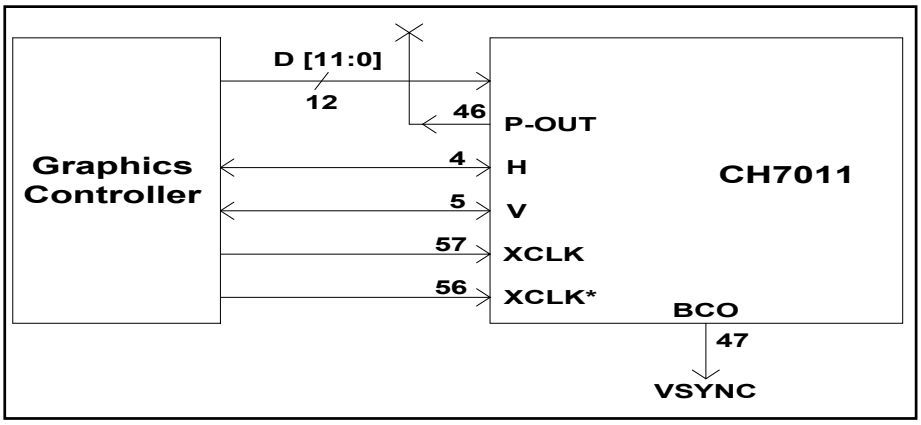


Figure 5: Slave Clock Mode

- **Embedded Sync Mode (TV-Out only)**

  In order to enable this mode, the Input Data Format Register, reg. 1Fh, needs to be set for IDF = 4. Since the HSYNC and VSYNC signals can be embedded into the data stream, the connections of the HSYNC and VSYNC pins are not required between the graphics controller and CH7011. Please refer CCIR656 for details on how the HSYNC and VSYNC, odd field & even field signals are generated within the data stream (See **Figure 6** for more design details for embedded sync in slave clock mode. Please note that the master clock mode can also be used.)

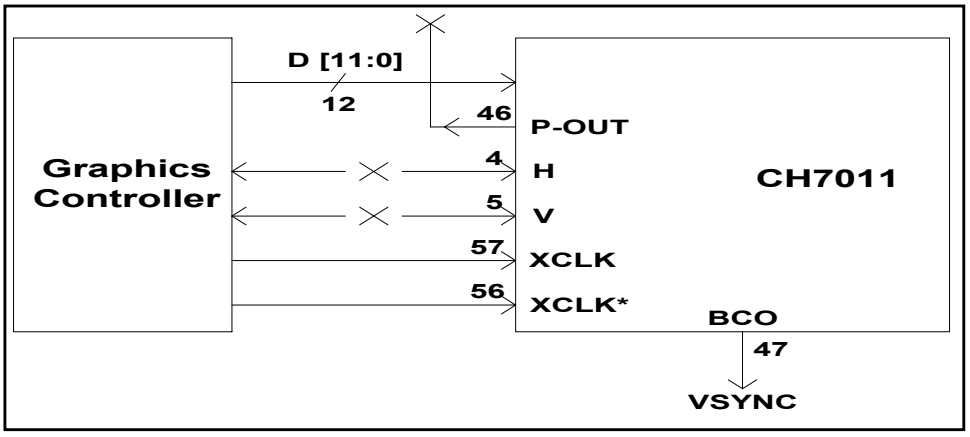


Figure 6: Embedded Sync (in slave clock) Mode

2.3 Clock and Crystal Oscillator

- **XI/FIN and XO pins**

  Crystal Input

  The 14.31818 MHz (±20ppm) crystal must be placed as close as possible to the XI/FIN and XO pins (pin 42 and pin 43), with traces connected from point to point, overlaying the ground plane. Since the crystal generates a timing reference for the CH7011 encoder, it is very important that noise should not couple into these input pins. Traces with fast edge rates should not be routed under or adjacent these pins. In addition, the ground reference of the external capacitors connected to the crystal pins must be connected very close to the CH7011 pin 41 ground (See **Figure 7**).

Reference Crystal Oscillator

The CH7011 includes an oscillator circuit which allows a 14.31818MHz crystal to be connected directly. Alternatively, an externally generated 14.31818MHz clock source may be supplied to the CH7011. If an external clock source is used, it should have CMOS level specifications. The clock should be connected to the XI/FIN pin, and the XO pin should be left open. The external source must exhibit ±20ppm or better frequency tolerance, and have low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

Crystal is specified to be 14.31818 MHz, ±20 ppm fundamental type and in parallel resonance (NOT series resonance). The crystal should also have a load capacitance equal to its specified value (C_L).

External load capacitors have their ground connection very close to the CH7011 (C_{ext}).

To allow tunability, a variable cap may be used from XI/FIN to ground.

Note that the XI/FIN and XO pin each has approximately 10 pF (C_{int}) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI/FIN and XO pins, the following calculation should be used:

$C_{ext} = (2 \times C_L) - C_{int} - 2C_S$

where:

C_{ext}= external load capacitance required on XI/FIN and XO pins.

C_L= crystal load capacitance specified by the crystal manufacturer.

C_{int}= capacitance internal to CH7011 (approximately 10-15 pF on each of XI/FIN and XO pins).

C_S= stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.).

Please refer to **Figure 7** for the symbols used in the calculation described above.

In general, let us assume

C_{int} XI/FIN = C_{int} XO = C_{int}

C_{ext} XI/FIN = C_{ext} XO = C_{ext}

such that

$C_L = (C_{int} + C\ ext) / 2 + C_S$ and **$C\ ext = 2 (C_L - C_S) - C_{int}$**

$= 2 C_L - (2C_S + C_{int})$

Therefore **C_L** must be specified greater than **$C_{int}/2 + C_S$** in order to select **C_{ext}** properly.

After C_L (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is not operating in excessive drive level specified by the crystal manufacturer. Otherwise, the crystal will age quickly and that in turn will affect the operating frequency of the crystal.

For the detail considerations of crystal oscillator design, please refer AN-06.

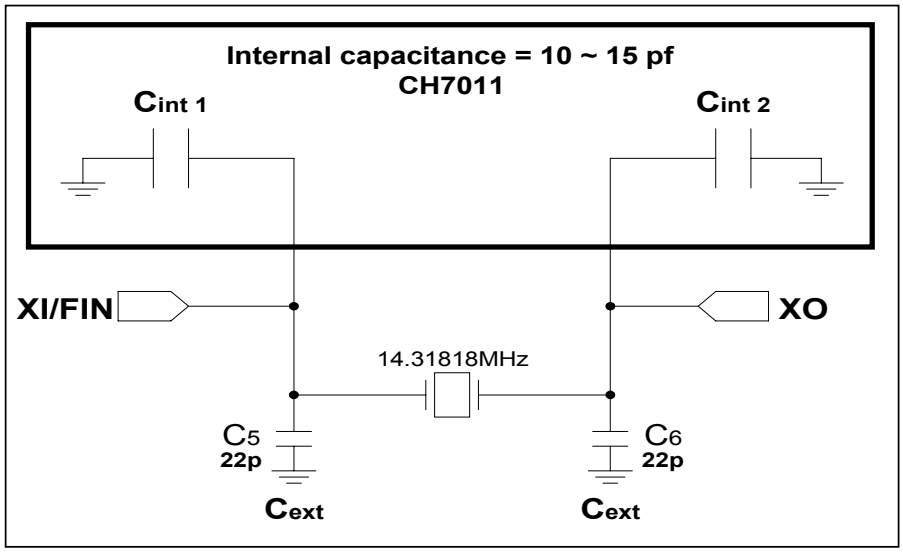


Figure 7: Reference Crystal Design

2.4 TV Video Outputs

In TV Output mode, multiplexed input data, sync and clock signals are input to the CH7011 from the graphics controller's digital output port. A P-OUT clock can be outputted as the reference frequency to the graphics controller, which is recommended to ensure accurate frequency generation. Horizontal and vertical sync signals are normally sent to the CH7011 from the graphics controller, but can be output to the graphics controller as an option (this is not recommended for pixel rates above 50MHz). Data will be 2X multiplexed, and the XCLK clock signal can be 1X or 2X times the pixel rate. The input data will be encoded into the selected video standard, and output from the video DACs. The modes supported for TV output are shown in **Table 3**.

Please beware that in order to minimize the hazard of ESD, a set of protection diodes MUST BE used for each DAC connecting to TV (Refer to AN-38 for details).

Table 3: TV Output Modes

Graphics Resolution	Active Aspect Ratio	Pixel Aspect Ratio	TV Output Standard	Scaling Ratios
512x384	4:3	1:1	PAL	5/4, 1/1
512x384	4:3	1:1	NTSC	5/4, 1/1
720x400	4:3	1.35:1.00	PAL	5/4, 1/1
720x400	4:3	1.35:1.00	NTSC	5/4, 1/1
640x400	8:5	1:1	PAL	5/4, 1/1
640x400	8:5	1:1	NTSC	5/4, 1/1, 7/8
640x480	4:3	1:1	PAL	5/4, 1/1, 5/6
640x480	4:3	1:1	NTSC	1/1, 7/8, 5/6
720x480[1]	4:3	9:8	NTSC	1/1
720x480[2]	4:3	9:8	NTSC	1/1, 7/8, 5/6
720x576[1]	4:3	15:12	PAL	1/1
720x576[2]	4:3	15:12	PAL	1/1, 5/6, 5/7
800x600	4:3	1:1	PAL	1/1, 5/6, 5/7
800x600	4:3	1:1	NTSC	3/4, 7/10, 5/8
1024x768	4:3	1:1	PAL	5/7, 5/8, 5/9
1024x768	4:3	1:1	NTSC	5/8, 5/9, 1/2

The components associated with the video output pins should be placed as close as possible to the CH7011. The 75Ω output termination, the output filter network, and the output connectors should be located as close as possible to the

CH7011 to minimize the noise pickup as well as possible reflections due to impedance mismatches. The video output signals should overlay the ground plane and should be routed away from digital lines that could introduce crosstalk. The Y and C outputs should be separated by a ground trace and inductors and ferrite beads in series with these outputs should not be located next to each other.

The recommended output reconstruction filter network is a third order low pass filter. The recommended circuit for a typical S-Video and Composite outputs are shown in **Figure 8**, and its corresponding frequency response is shown in **Figure 9** and **Figure 10**.

Careful layout consideration for the CVBS, Y/G, C/R & CVBS/B traces and the attached components are needed in order to avoid coupling among each other. It is suggested that the signal traces of Y, C and CVBS be separated with ground traces and routed to the connectors. Also, the capacitors and the inductors attached to those outputs should not placed too close to each other.

The CVBS, Y/G, C/R & CVBS/B signals are analog video signals. These signals should be routed using 75Ω traces. These signals should not be routed together. There should be a minimum of 12 mils spacing between each of the these signals and 20 mils spacing between them and any other digital trace.

Typically these signals should be routed in a separate analog area without any digital signals running through the area. Corners for these traces should be at a maximum of 45 degree. 90 degree corner should not be used due to cross coupling between adjacent traces. These traces should be kept on the top layer to minimize the use of vias on them.

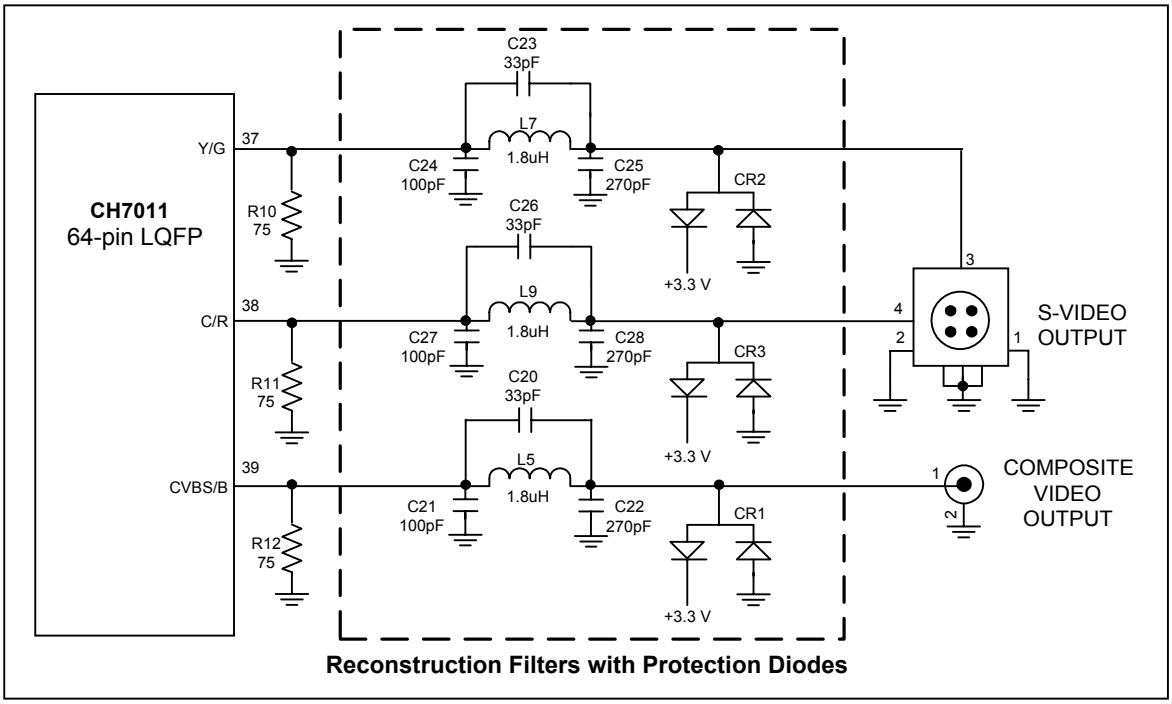


Figure 8: The Typical Connection For the S-Video and Composite Outputs

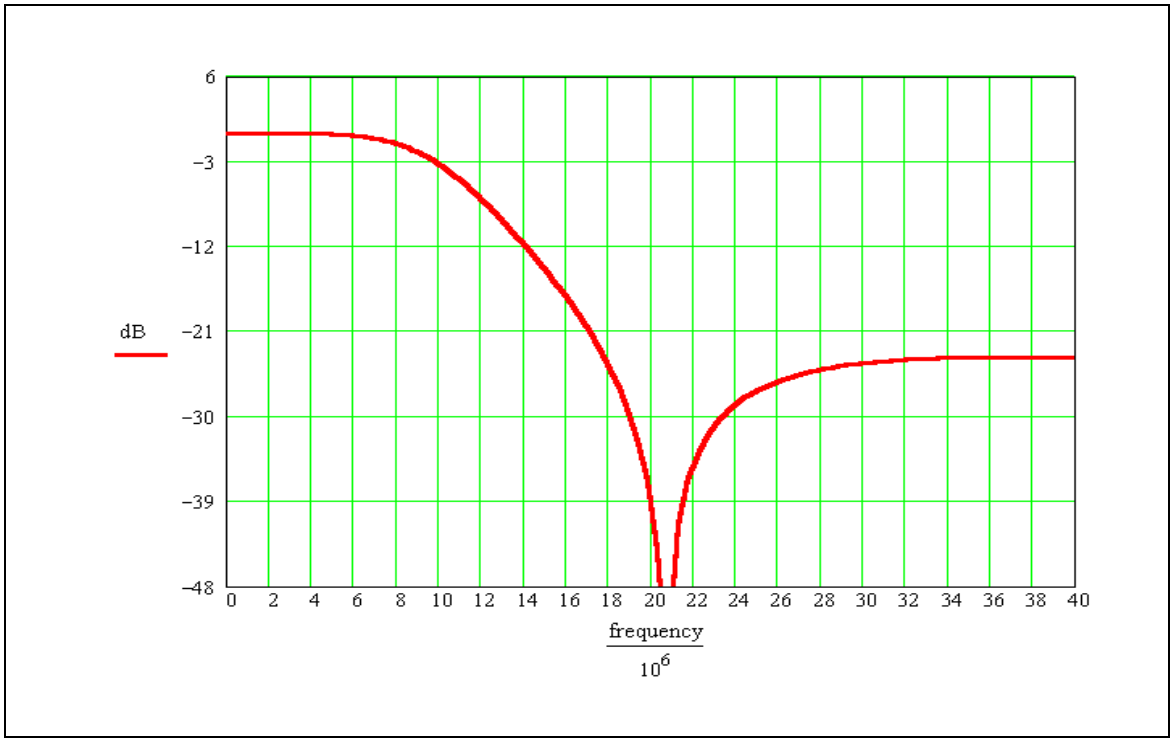


Figure 9: S-video and Composite Output Amplitude Response of the 3rd Order Reconstruction Filter as shown in Figure 8

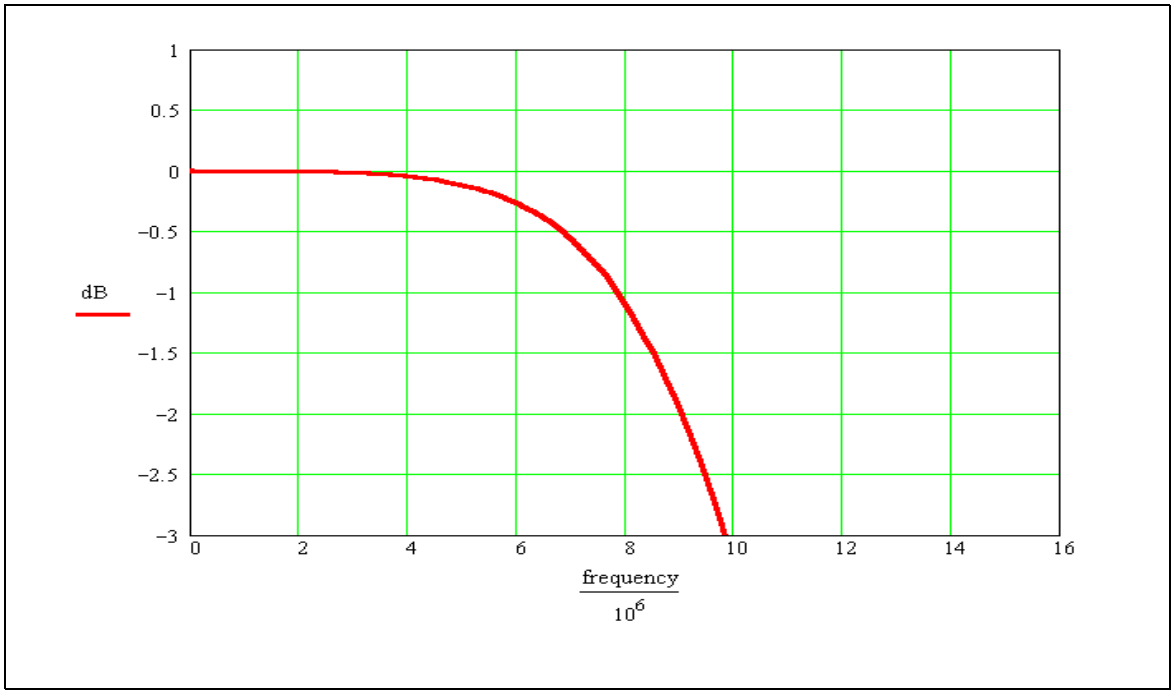


Figure 10: The Details of the Amplitude Response of the Pass Band

Note: If the application only allows one video output connection and simultaneously display of S-Video and Composite is not needed, please refer AN27 on how to achieve the desire configuration.

SCART arrangements 1 and 2 can be achieved using the layout scheme shown in **Figure 11**. Using this layout, the SCART arrangement type can be chosen by means of register changes. For SCART arrangement 1, set FF Register (address 01h) bit 6 VOF = 1 and BL Register (address 07h) BL[7:0] = 0. For SCART arrangement 2, set VOF = 0 and BL[7:0] = 110, and CVBWB =0 (Register 02h bit 5).

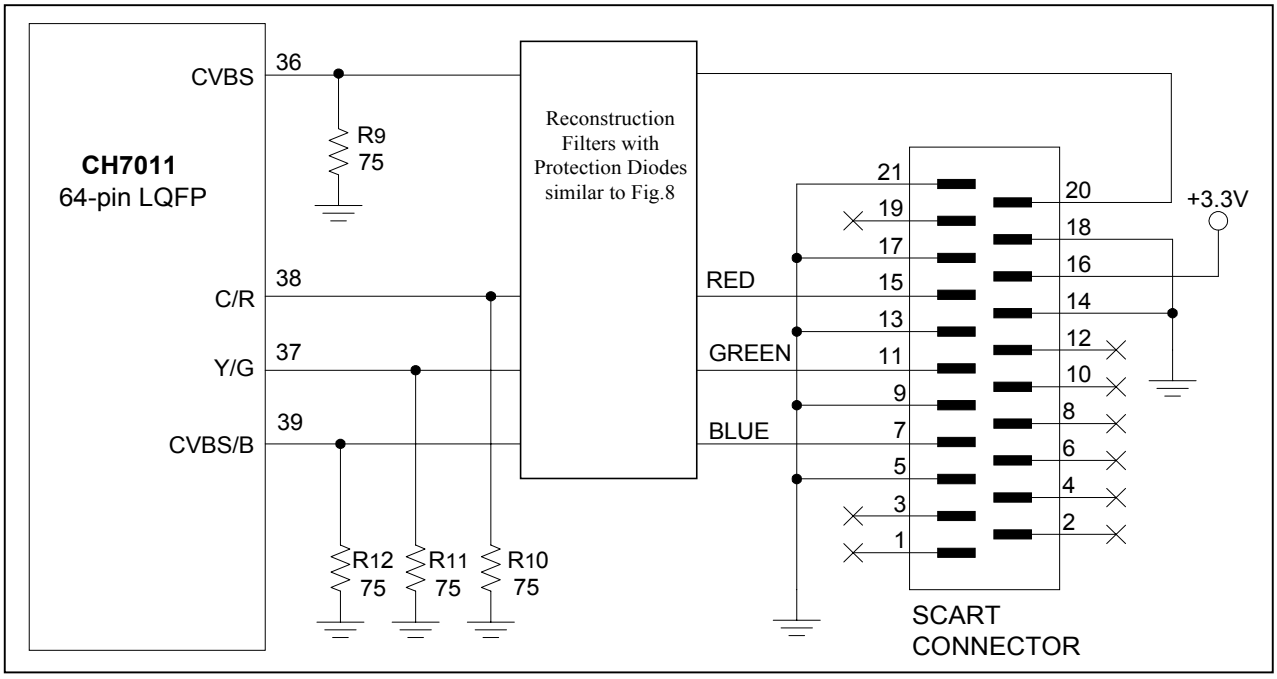
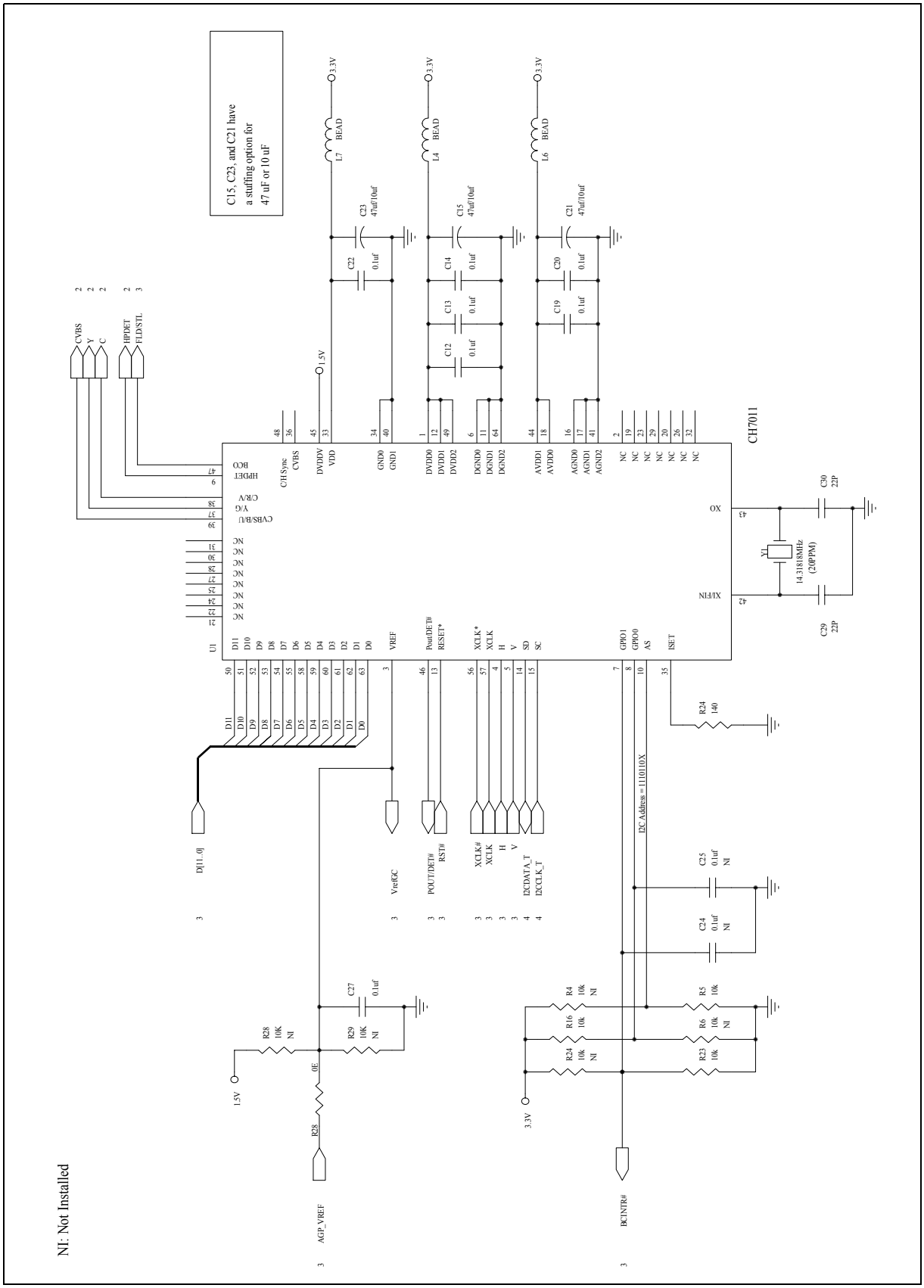


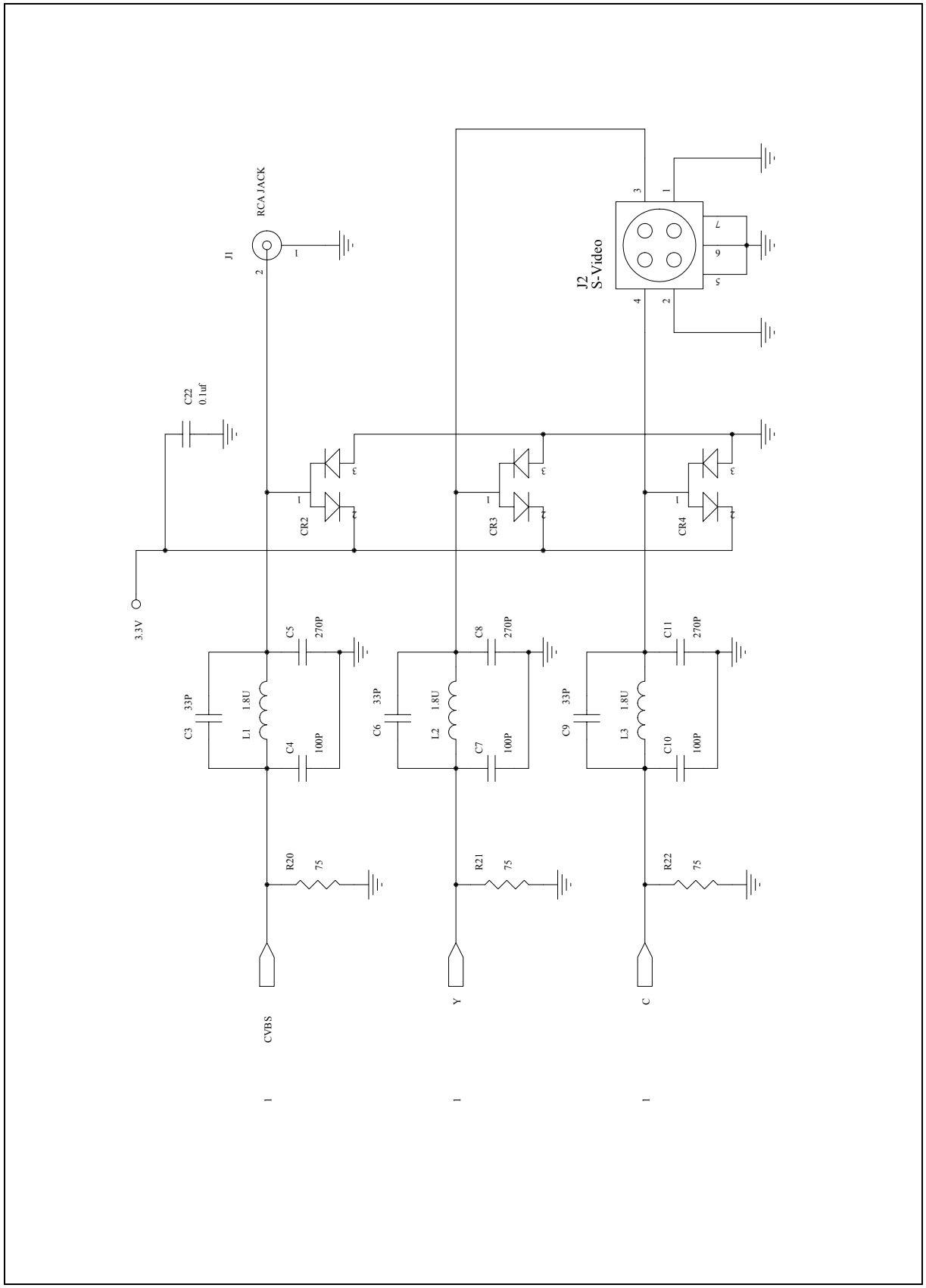
Figure 11: The Connection for SCART Arrangements 1 and 2

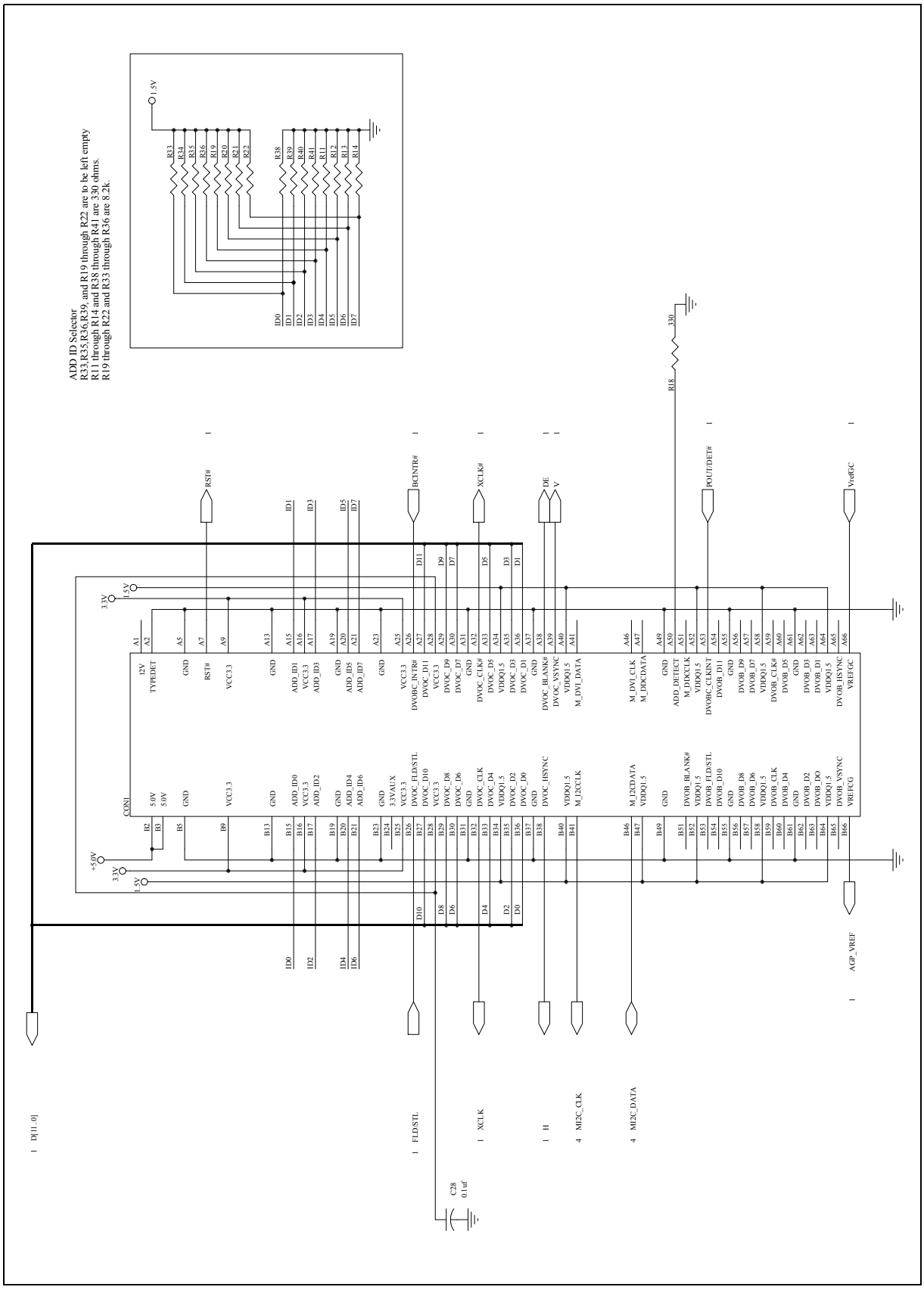
3. Reference Design Example

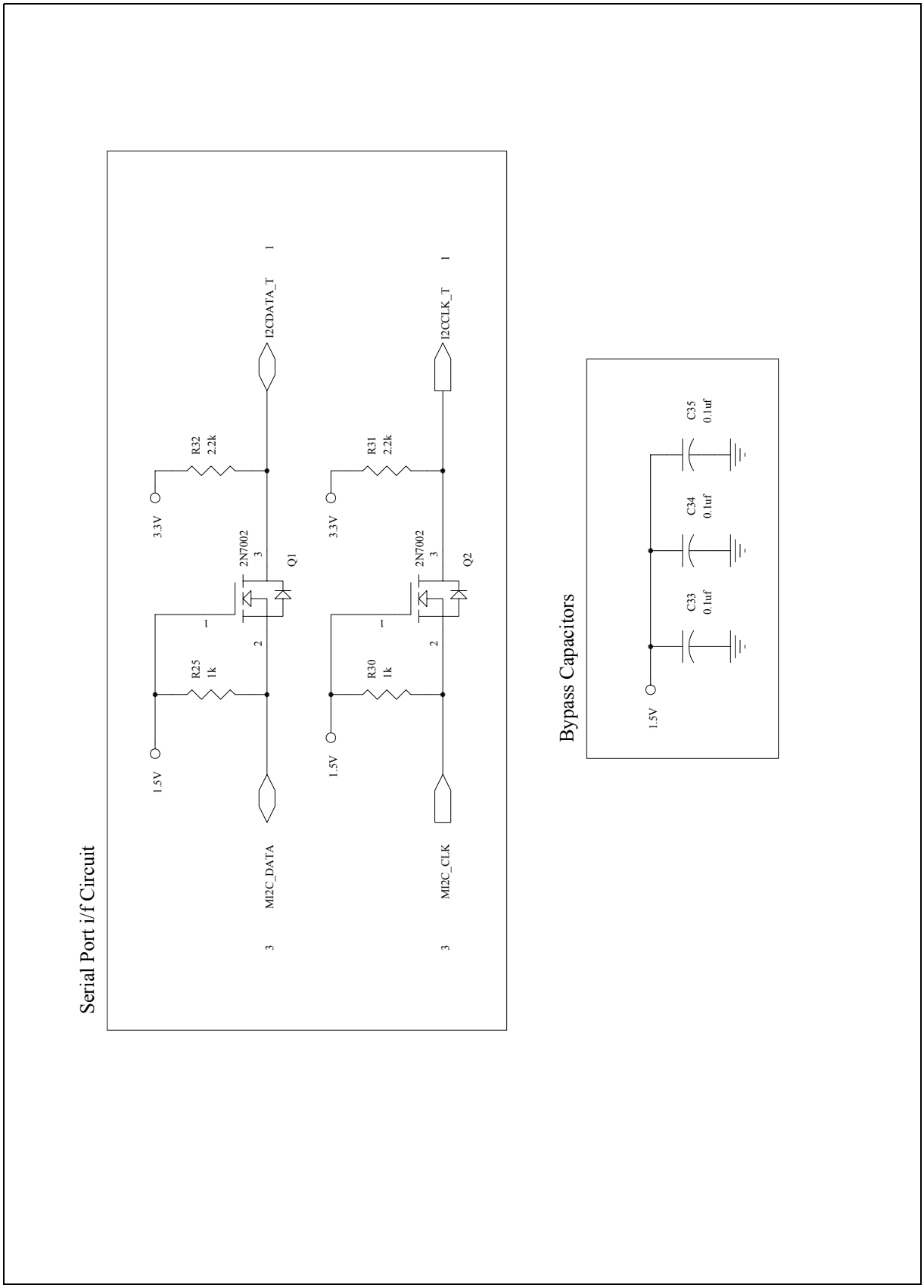
The following schematics are based on an Intel Brookdale® / Montara® / Springdale® Graphics chipset design and are to be used as a CH7011 PCB design example only. It is not a complete design. Those who are seriously doing an application design with the CH7011 and would like to have a complete reference design schematic, should contact Applications within Chrontel, Inc.

3.1 Schematics of Reference Design Example


C15, C23, and C21 have
a stuffing option for
47 uF or 10 uF
CH7011
U1
NI: Not Installed
I2C Address = 1110110X
D[11..0]
VrefGC
POUT/DET#
RST#
XCLK#
XCLK
H
V
I2CDATA_T
I2CCLK_T
AGP_VREF
BCINTR#
CVBS
Y
C
HPDET
FLDSTL
3.3V
1.5V
L7 BEAD
L4 BEAD
L6 BEAD
C23 47uF/10uF
C15 47uF/10uF
C21 47uF/10uF
C22 0.1uf
C14 0.1uf
C13 0.1uf
C12 0.1uf
C20 0.1uf
C19 0.1uf
C30 22P
C29 22P
Y1
14.31818MHz
(20PPM)
R24 140
C25 0.1uf NI
C24 0.1uf NI
C27 0.1uf
R28 10K NI
R29 10K NI
R28 0E
R4 10k NI
R5 10k
R16 10k
R6 10k NI
R24 10k NI
R23 10k


J1
RCA JACK
J2
S-Video
C22
0.1uf
3.3V
CR2
CR3
CR4
C3 33P
L1 1.8U
C4 100P
C5 270P
C6 33P
L2 1.8U
C7 100P
C8 270P
C9 33P
L3 1.8U
C10 100P
C11 270P
R20 75
R21 75
R22 75
CVBS
Y
C


ADD ID Selector
R33,R35,R36,R39, and R19 through R22 are to be left empty
R11 through R14 and R38 through R41 are 330 ohms.
R19 through R22 and R33 through R36 are 8.2k.
1.5V
R23
R34
R35
R36
R19
R20
R21
R22
R38
R39
R40
R41
R11
R12
R13
R14
ID0
ID1
ID2
ID3
ID4
ID5
ID6
ID7
330
R18
RST#
BCINTR#
XCLK#
DE
V
POUT/DET#
VrefGC
CON1
I2V
TYPEDET
GND
RST#
VCC3.3
ADD_ID1
ADD_ID3
ADD_ID5
ADD_ID7
DVOBC_INTR#
DVOC_D11
DVOC_D9
DVOC_D7
DVOC_CLK#
DVOC_D5
DVOC_D3
DVOC_D1
DVOC_BLANK#
DVOC_VSYNC
M_DVI_DATA
M_DVI_CLK
M_DDCDATA
ADD_DETECT
M_DDCCLK
VDDQ1.5
DVOBC_CLKINT
DVOB_D11
DVOB_D9
DVOB_D7
DVOB_CLK#
DVOB_D5
DVOB_D3
DVOB_D1
DVOB_HSYNC
VREFGC
ADD_ID0
ADD_ID2
ADD_ID4
ADD_ID6
3.3VAUX
DVOC_FLD/STL
DVOC_D10
DVOC_D8
DVOC_D6
DVOC_CLK
DVOC_D4
DVOC_D2
DVOC_D0
DVOC_HSYNC
M_I2CCLK
M_I2CDATA
DVOB_BLANK#
DVOB_FLD/STL
DVOB_D10
DVOB_D8
DVOB_D6
DVOB_CLK
DVOB_D4
DVOB_D2
DVOB_D0
DVOB_VSYNC
+5.0V
3.3V
1.5V
D10
D8
D6
D4
D2
D0
C28
0.1uf
1 D[11..0]
1 FLD/STL
1 XCLK
1 H
4 M2C_CLK
4 M2C_DATA
1 AGP_VREF


Serial Port i/f Circuit
3.3V
R32
2.2k
I2CDATA_T
1
2N7002
3
Q1
1.5V
R25
1k
2
1
3
MI2C_DATA
3.3V
R31
2.2k
I2CCLK_T
1
2N7002
3
Q2
1.5V
R30
1k
2
1
3
MI2C_CLK
Bypass Capacitors
1.5V
C33
0.1uf
C34
0.1uf
C35
0.1uf

4. Revision History

Revision	Date	Section	Description
1.0	4/11/00	All	First official release, revision 1.0
1.1	9/29/00	General Controls and Inputs	Figure 7 Updated.
1.2	2/5/02	General Controls and Inputs	ESD protection diode recommendation note added.
2.0	1/30/03	All	All Figures and Tables updated.
		3.0	Reference schematics updated to an Intel Bookdale® / Montara® / Springdale® reference design.

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