TV-Out Connection with CRT Discharge Protection

Introduction

This application note is applicable to 70xx and 720x (S-Video, Composite and SCART Video) family. This recommendation takes precedence over the same information presented in the datasheets.

It provides a suggestion on how to make a correct connection to S-Video, Composite or SCART connector of a TV with a protection to the encoder device from the CRT discharge of the TV.

Due to CRT discharge from the TV, the signal lead might have +ve or -ve voltage surge. To protect the DACs inside the device, two diodes are connected to each output signal Y, C, and CVBS as shown in the circuit below.

This discharge protection is achieved by using two diodes either 1N34A (Germanium) or 1N44 (Silicon) each, one connected to Vdd and the other connected to GND. They are placed as close to the connectors as possible so that they are turned on earlier than the internal diode protection circuit. In case of +ve voltage surge, the diode connected to Vdd is turned on and in case of -ve surge, the diode connected to GND is turned on providing the proper discharge of the voltage.

Figures 1 and 2 show the reference design for S-Video and Composite Video outputs.

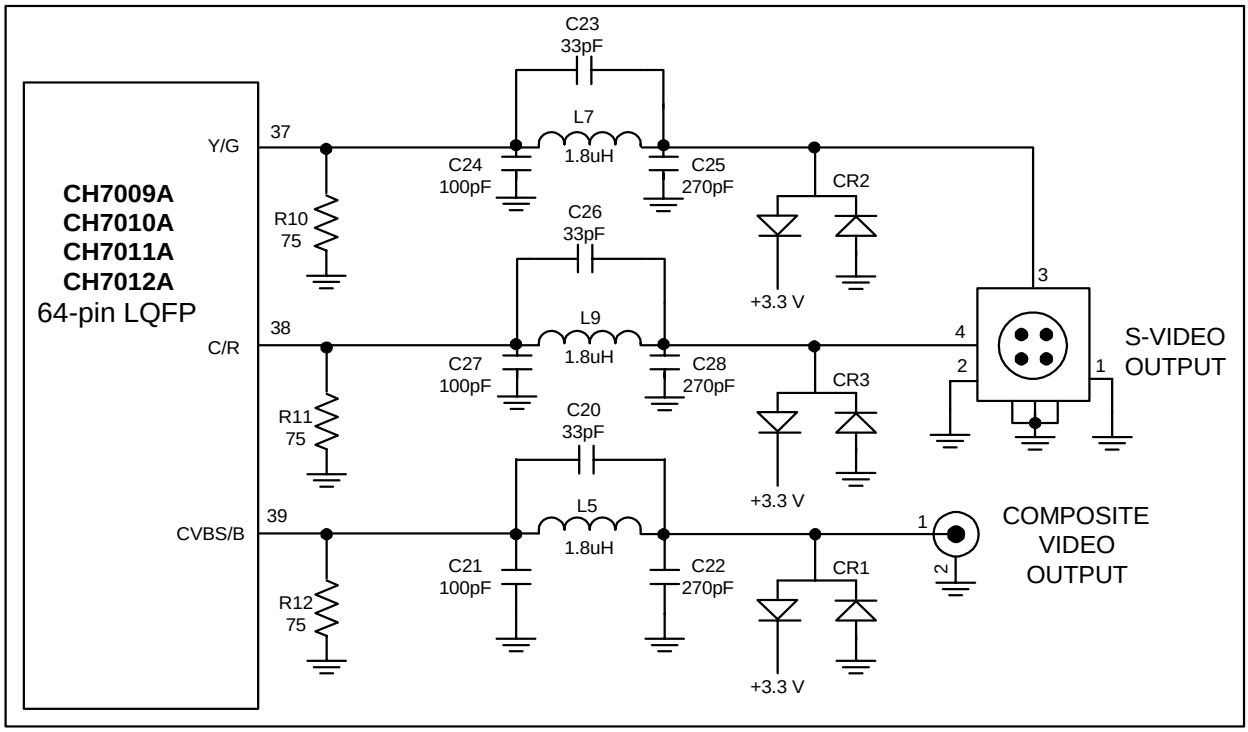

Figure 1: S-Video and Composite Video Outputs

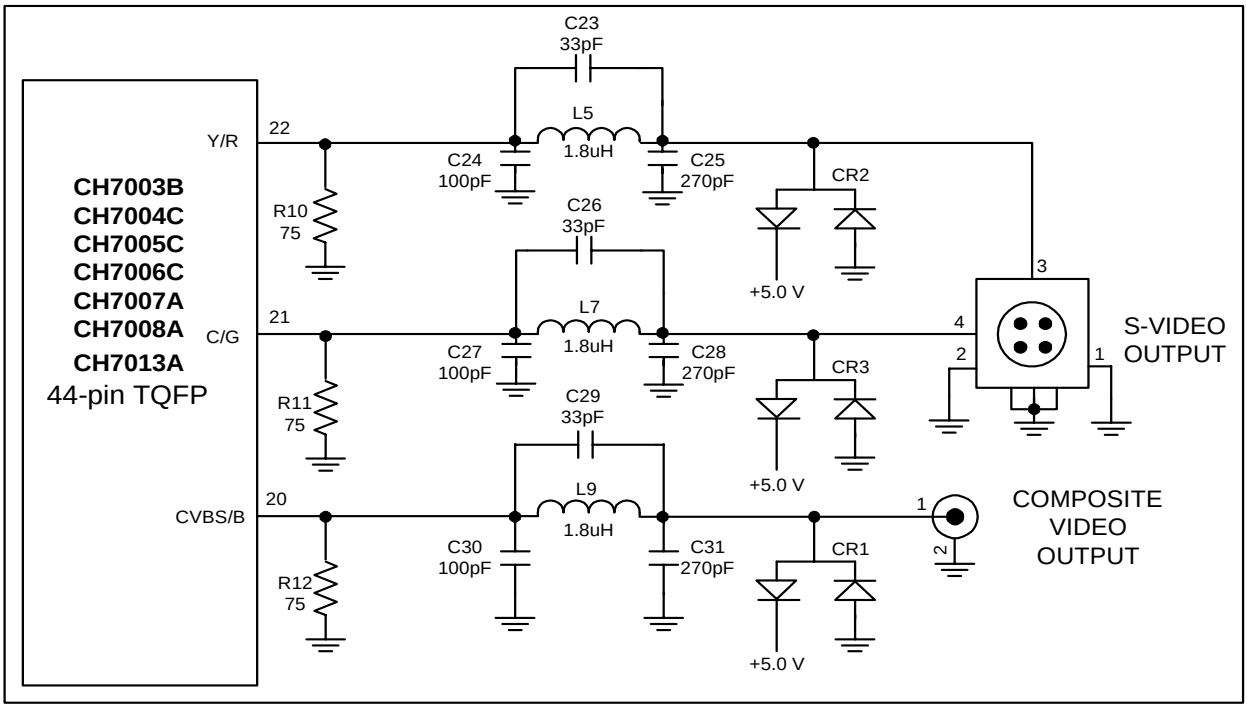

Figure 2: S-Video and Composite Video Outputs

Figures 3 to 6 show the reference design for SCART Outputs.

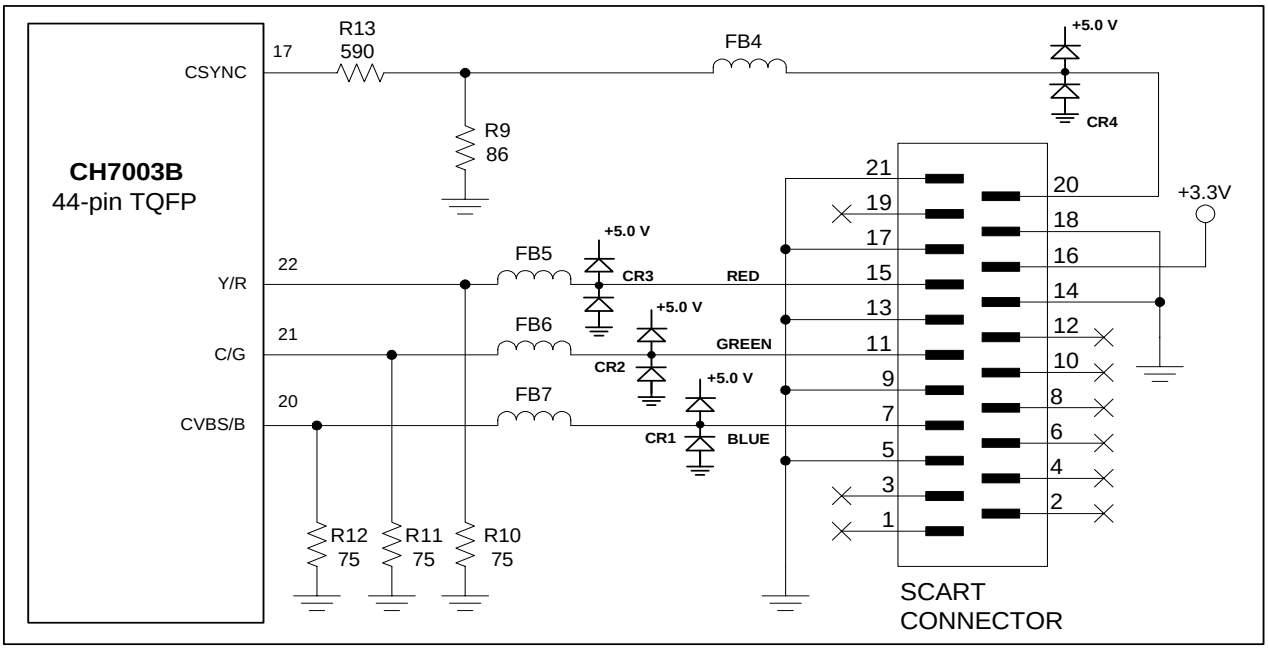

Figure 3: SCART type I Video Output

R13 and R9 set the peak voltage level at R9 to be around 0.4 V. This is used for the composite sync in SCART mode. The equivalent resistance at the node of R9 should be as close to 75 ohms as possible. Please note that there is a flexibility to select standard resistor values for R13 and R9.

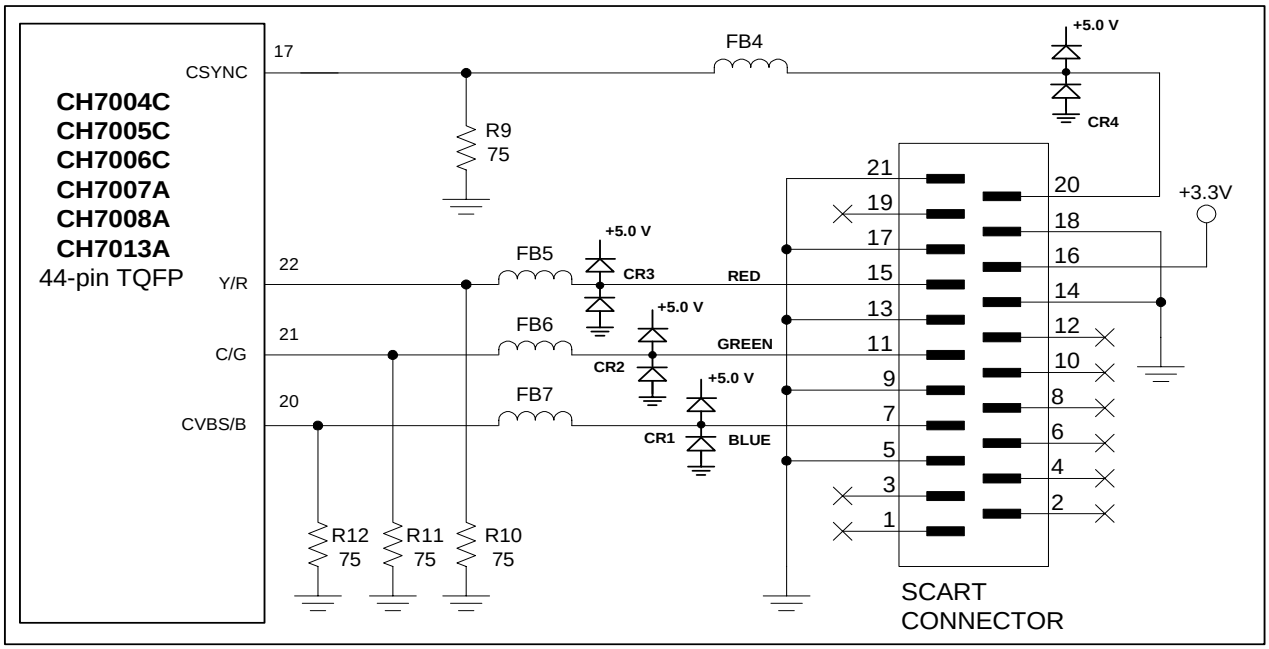

Figure 4: SCART type I Video Output

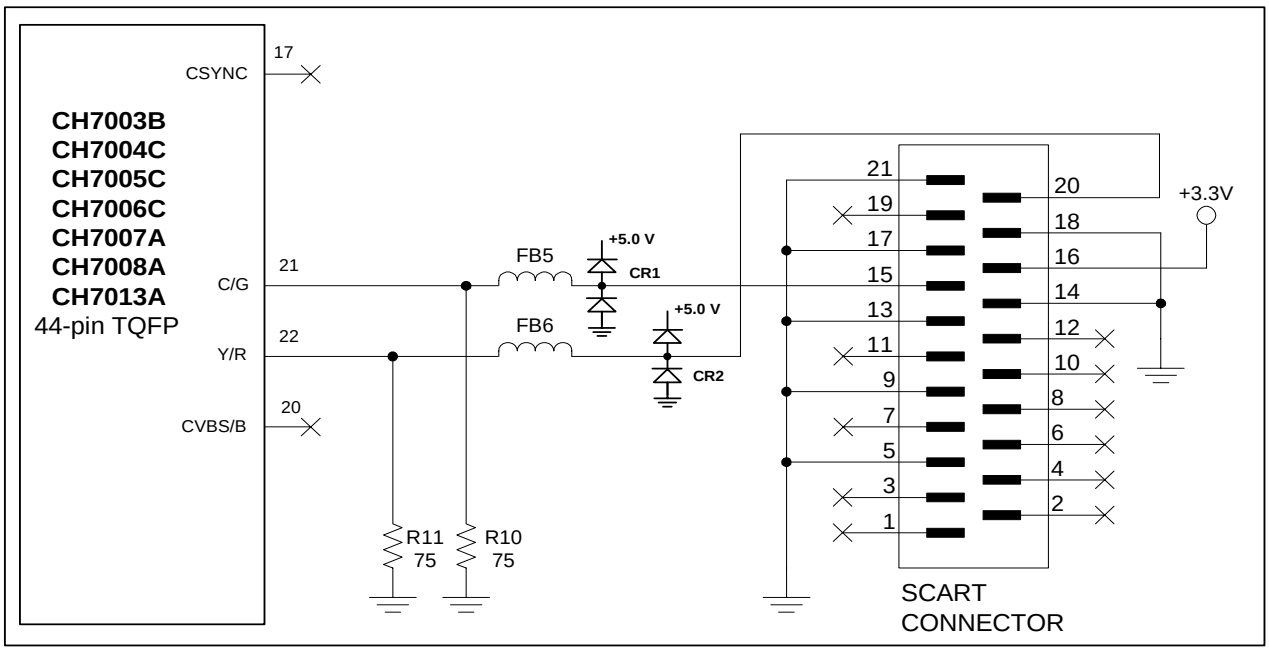

Figure 5: SCART type II Video Output

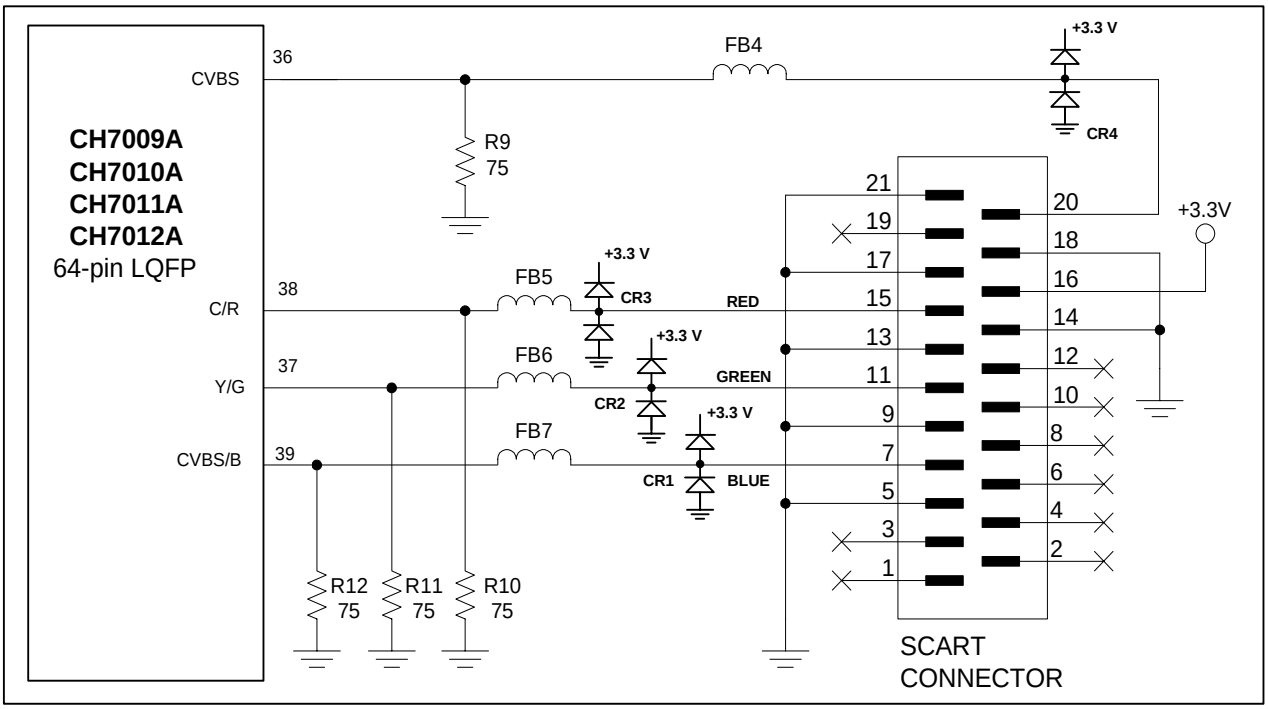

Figure 6: SCART Video Output

For CH7009, CH7010, CH7011 and CH7012. This schematic can support both SCART type I and type II. For SCART arrangement 1, set FF Register (address 01h) bit 6 VOF = 1 and BL Register (address 07h) BL[7:0] = 0. For SCART arrangement 2, set VOF = 0 and BL[7:0] = 110, and CVBWB =0 (Register 02h bit 5).