CH7009 Family Encoder Registers Read/Write Operation

Introduction

The CH7009 family (CH7009, CH7010, CH7011, CH7012, CH7301) contains a serial port, through which the control registers can be written and read. This port has a two-wire serial interface, Pins SPD (bidirectional) - Serial Port Data, and SPC - Serial Port Clock.

The serial port clock line (SPC) is input only and is driven by the output buffer of the graphics controller device, which is the clock master in the system. The serial port data line (SPD) is either input to or output from CH7009 family encoder depending on the write or read status. The data on the bus can be transferred up to 400 kbit/s. **Figure 1** shows the connection of the serial port interface of CH7009 family.

Please note that we DO NOT recommend sharing of this serial port with other serial port programmable devices.

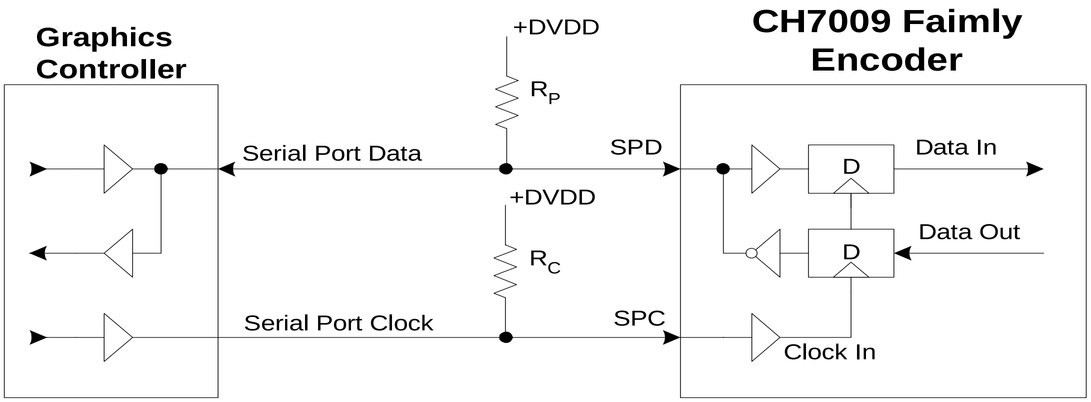


Figure 1: The Connection of the Serial Port Interface of CH7009 Family Encoder.

Serial Port Operation

Electrical Characteristics of the Serial Port

The connections of the serial port inputs and outputs are shown in **Figure 1**. A pull-up resistor (R_P) must be connected to a 3.3V ± 10% supply. The CH7009 family encoder is a device with input levels related to DVDDV.

A weak pull-up resister (R_C) may be added to the clock line to ensure that it is pulled high when the bus is free.

Maximum and minimum values of pull-up resistor (R_P)

The value of R_P depends on the following parameters:

- Supply voltage
- Bus capacitance
- Number of devices connected (input current + leakage current = I_{input})

The supply voltage limits the minimum value of resistor R_P due to the specified minimum sink current of 2mA at VOL_{max} = 0.4 V for the output stages:

$$R_P >= (V_{DD} – 0.4) / 2 \quad (R_P \text{ in } k\Omega)$$

The line capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of R_P due to the specified rise time. The equation for R_P is shown below:

$$R_P <= 10^3/C \quad \text{(where: } R_P \text{ is in } k\Omega \text{ and C, the total capacitance, is in pF)}$$

The maximum HIGH level input current of each input/output connection has a specified maximum value of 10 µA. Due to the desired noise margin of $0.2V_{DD}$ for the HIGH level, this input current limits the maximum value of R_P. The R_P limit depends on V_{DD} and is shown below:

$$R_P <= (100 \text{ x } V_{DD})/ I_{input} \quad \text{(where: } R_P \text{ is in } k\Omega \text{ and } I_{input} \text{ is in } \mu A)$$

Transfer Protocol

Both read and write cycles can be executed in “Auto-increment” or “Single-step” modes. Auto-increment mode allows you to establish the initial register location, then automatically increments the register address after each subsequent data access (i.e., transfers will be address, data...). The Single-step mode, as a matter of fact, is the Auto-increment mode with a single set of data sending/receiving to/from a specific register. A basic serial port transfer protocol is shown in **Figure 2** and is described below.

Please note that CH7009 family encoders DO NOT support “Alternating Mode”, which is supported by CH7007/CH7008 encoders.

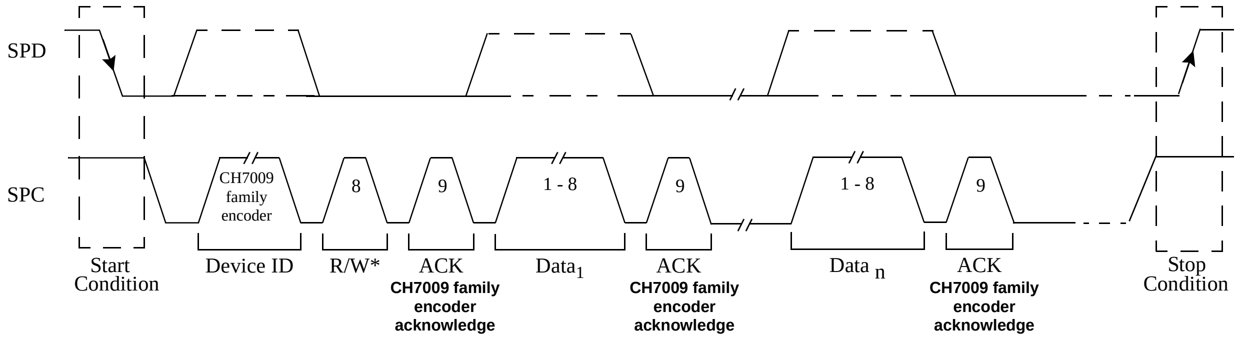


Figure 2: Serial Port Transfer Protocol

Transfer Protocols *(continued)*

1. The transfer sequence is initiated when a high-to-low transition of SPD occurs while SPC is high; this is the “START” condition. Transitions of address and data bits can only occur while SPC is low.
2. The transfer sequence is terminated when a low-to-high transition of SPD occurs while SPC is high; this is the “STOP” condition.
3. Upon receiving the first START condition, the CH7009 family encoder expects a Device Address Byte (DAB) from the master device. The value of the device address is shown in the DAB data format below (when AS = 1, it is EAh/EBh, when AS = 0, it is ECh/EDh).
4. After the DAB is received, the CH7009 family encoder expects a Register Address Byte (RAB) from the master. The format of the RAB is shown in the RAB data format below (note that B7 is not used).

Device Address Byte (DAB)

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	1	AS*	AS	R/W

R/W **Read/Write Indicator**

“0”: master device will write to the CH7009 family encoder at the register location specified by the address AR[6:0]

“1”: master device will read from the CH7009 family encoder at the register location specified by the address AR[6:0].

Register Address Byte (RAB)

B7	B6	B5	B4	B3	B2	B1	B0
1	AR[6]	AR[5]	AR[4]	AR[3]	AR[2]	AR[1]	AR[0]

AR[6:0] **Specifies the Address of the Register to be Accessed.**

This register address is loaded into the Address Register of the CH7009 family encoder. The R/W access, which follows, is directed to the register specified by the content stored in the Address Register.

The following two sections describe the operation of the serial interface for the four combinations of R/W = 0,1 and Auto-increment and Single-step operation.

CH7009 Family Encoder Write Cycle Protocols (R/W = 0)

Data transfer with acknowledge is required. The acknowledge-related clock pulse is generated by the master-transmitter. The master-transmitter releases the SPD line (HIGH) during the acknowledge clock pulse. The slave-receiver must pull down the SPD line, during the acknowledge clock pulse, so that it remains stable LOW during the HIGH period of the clock pulse. The CH7009 family encoder always acknowledges for writes (see **Figure 3**). Note that the resultant state on SPD is the wired-AND of data outputs from the transmitter and receiver.

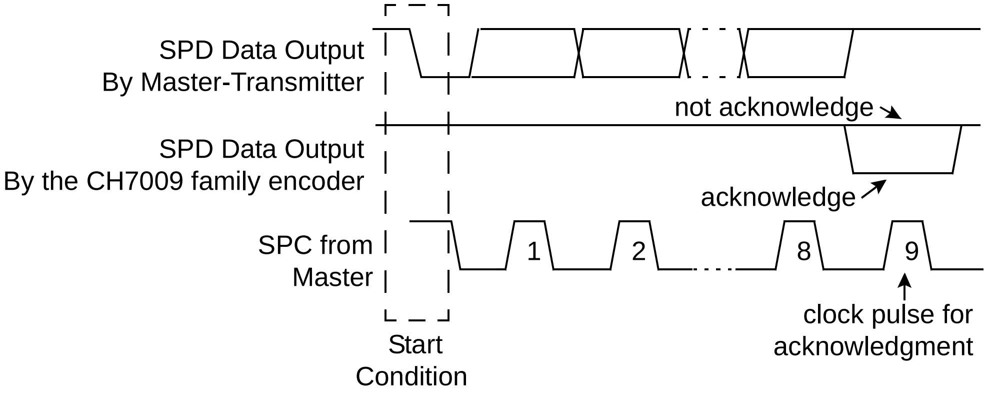
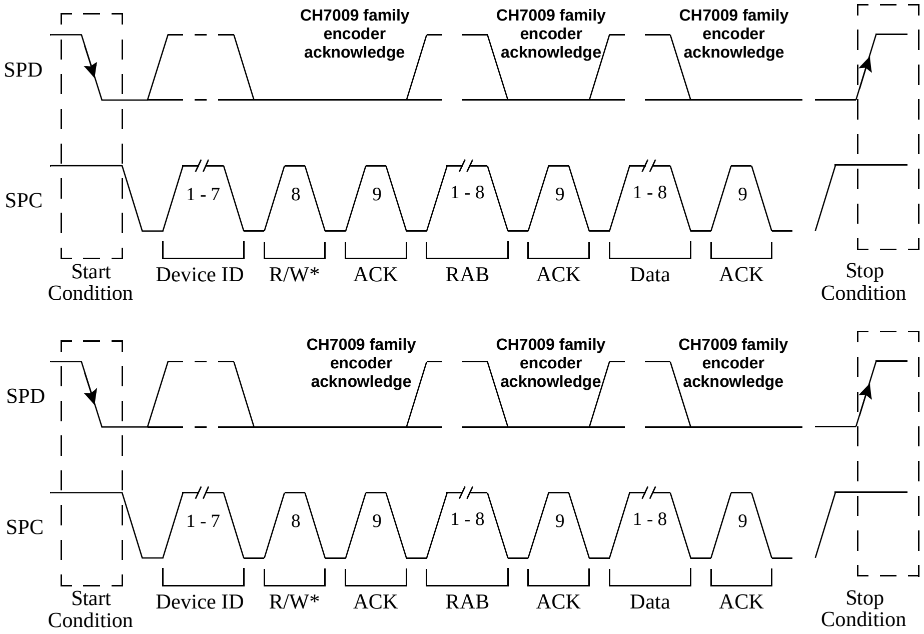


Figure 3: Acknowledge on the Bus

Figure 4 shows two consecutive Single step write cycles. The byte of information, following the Register Address Byte (RAB), is the data to be written into the register specified by AR[6:0] and the line go to "Stop Condition" immediately after the acknowledgment is received. The cyle is them repeated and so on.


CH7009 family encoder acknowledge
CH7009 family encoder acknowledge
CH7009 family encoder acknowledge
SPD
SPC
1 - 7
8
9
1 - 8
9
1 - 8
9
Start Condition
Device ID
R/W*
ACK
RAB
ACK
Data
ACK
Stop Condition
CH7009 family encoder acknowledge
CH7009 family encoder acknowledge
CH7009 family encoder acknowledge
SPD
SPC
1 - 7
8
9
1 - 8
9
1 - 8
9
Start Condition
Device ID
R/W*
ACK
RAB
ACK
Data
ACK
Stop Condition

Note: The acknowledge is from the CH7009 family encoder (slave).

Figure 4: Single-step Write Cycles (2 cycles)

An Auto-increment write cycle is shown in **Figure 5**. During the Auto-increment mode transfers, the register address pointer continues to increment for each data write cycle until AR[6:0] = 4F. The next byte of information represents a new auto-sequencing “Starting address”, which is the address of the register to receive the next byte. The auto-sequencing then resumes based on this new “Starting address”. The Auto-increment sequence can be terminated any time by either a “STOP” or “RESTART” condition. The write operation can be terminated with a “STOP” condition.

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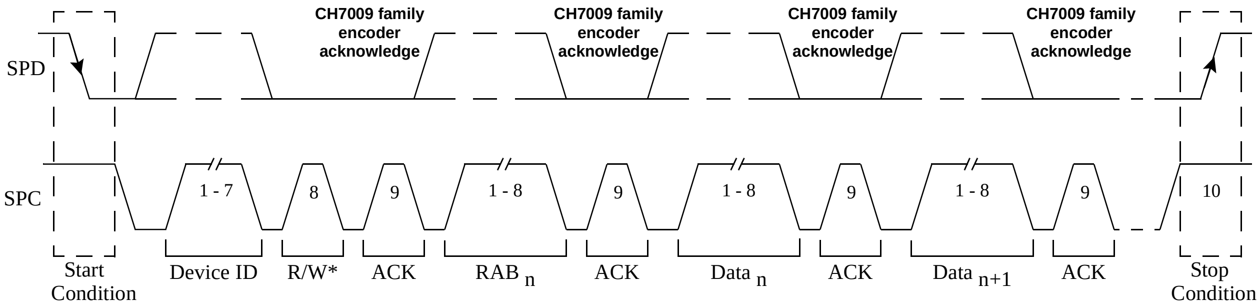
CH7009 family encoder acknowledge
CH7009 family encoder acknowledge
CH7009 family encoder acknowledge
CH7009 family encoder acknowledge
SPD
SPC
1 - 7
8
9
1 - 8
9
1 - 8
9
1 - 8
9
10
Start Condition
Device ID
R/W*
ACK
RAB n
ACK
Data n
ACK
Data n+1
ACK
Stop Condition

Note: The acknowledge is from the CH7009 family encoder (slave).

Figure 5: Auto-Increment Write Cycle

CH7009 Family Encoder Read Cycle Protocols (R/W = 1)

If a master-receiver is involved in a transfer, it must signal the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter CH7009 family encoder releases the data line to allow the master to generate the STOP condition or the RESTART condition.

To read the content of the registers, the master device starts by issuing a “START” condition (or a “RESTART” condition). The first byte of data, after the START condition, is a DAB with R/W = 0. The second byte is the RAB with AR[6:0], containing the address of the register that the master device intends to read from in AR[6:0]. The master device should then issue a “RESTART” condition (“RESTART” = “START”, without a previous “STOP” condition). The first byte of data, after this RESTART condition, is another DAB with R/W=1, indicating the master’s intention to read data hereafter. The master then reads the next byte of data (the content of the register specified in the RAB). For Single-step mode, a “Stop” condition or “Restart” condition is sent out immediately after the acknowledge of data read (see **Figure 6**).

Transfer Protocols *(continued)*

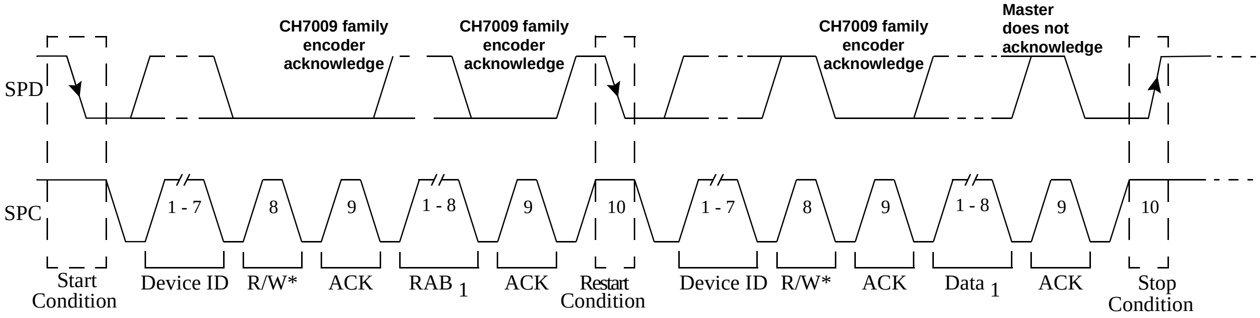

Figure 6: Single-step Read Cycle

For Auto-increment read cycle, the address register will be incremented automatically and subsequent data bytes can be read from successive registers without providing a second RAB.

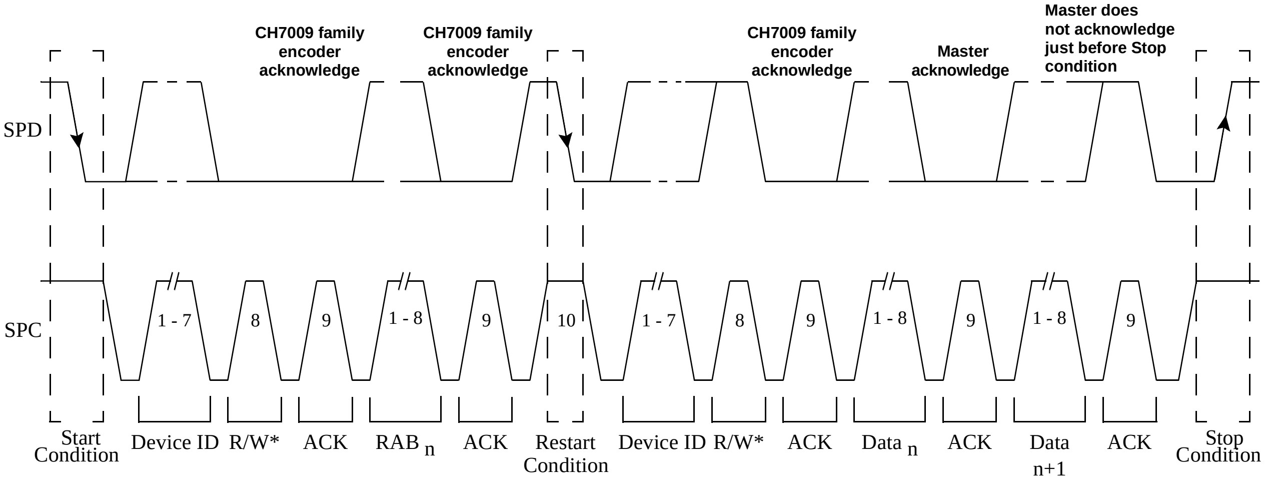

Figure 7: Auto-increment Read Cycle

Regarding the Auto-increment mode, the address register continues to increment for each read cycle. When the content of the address register reaches 4Fh, it will wrap around and start from 00h again. The auto increment sequence can be terminated by either a “STOP” or “RESTART” condition. The read operation can be terminated with a “STOP” condition. **Figure 7** shows an Auto-increment read cycle terminated by a STOP condition.

Registers Map of CH7009 Family Encoders

Table 1 shows the non-Macrovision registers map of CH7009 family encoders.

Table 1: CH7009 Family Encoder non-Macrovision Registers Map

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	IR2	IR1	IR0	VOS1	VOS0	SR2	SR1	SR0
01h		VOF0	CFF1	CFF0	YFFT1	YFFT0	YFFNT1	YFFNT0
02h	VBID	CFRB	CVBWB	CBW	YSV1	YSV0	YCV1	YCV0
03h			SAV8	HP8	VP8	TE2	TE1	TE0
04h	SAV7	SAV6	SAV5	SAV4	SAV3	SAV2	SAV1	SAV0
05h	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
06h	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
07h	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
08h						CE2	CE1	CE0
09h	MEM2	MEM1	MEM0	N9	N8	M8	PLLCPI	PLLCAP
0Ah	M7	M6	M5	M4	M3	M2	M1	M0
0Bh	N7	N6	N5	N4	N3	N2	N1	N0
0Ch	FSCI31	FSCI30	FSCI29	FSCI28	FSCI27	FSCI26	FSCI25	FSCI24
0Dh	FSCI23	FSCI22	FSCI21	FSCI20	FSCI19	FSCI18	FSCI17	FSCI16
0Eh	FSCI15	FSCI14	FSCI13	FSCI12	FSCI11	FSCI10	FSCI9	FSCI8
0Fh	FSCI7	FSCI6	FSCI5	FSCI4	FSCI3	FSCI2	FSCI1	FSCI0
10h			CIV25	CIV24	CIVC1	CIVC0	PALN	CIVEN
11h	CIV23	CIV22	CIV21	CIV20	CIV19	CIV18	CIV17	CIV16
12h	CIV15	CIV14	CIV13	CIV12	CIV11	CIV10	CIV9	CIV8
13h	CIV7	CIV6	CIV5	CIV4	CIV3	CIV2	CIV1	CIV0
1Ch					M/S*	MCP	PCM	XCM
1Dh					XCMD3	XCMD2	XCMD1	XCMD0
1Eh	GOENB1	GOENB0	GPIOL1	GPIOL0	HPIR	HPIE	POUTE	POUTP
1Fh	IBS	DES	SYO	VSP	HSP	IDF2	IDF1	IDF0
20h	HPIE2	XOSC2	DVIT	DACT3	DACT2	DACT1	DACT0	SENSE
21h	XOSC1	XOSC0		SYNCO1	SYNCO0	DACG1	DACG0	DACBP
22h	SHF2	SHF1	SHF0	BCOEN	BCOP	BCO2	BCO1	BCO0
31h	TPPD3	TPPD2	TPPD1	TPPD0	CTL3	CTL2	CTL1	CTL0
32h	TPVCO7	TPVCO6	TPVCO5	TPVCO4	TPVCO3	TPVCO2	TPVCO1	TPVCO0
33h	DVID2	DVID1	DVID0	DVII			TPCP1	TPCP0
35h			TPVT5	TPVT4	TPVT3	TPVT2	TPVT1	TPVT0
36h	TPLPF3	TPLPF2	TPLPF1	TPLPF0				
37h	TPVCO10	TPVCO9	TPVCO8					
48h				ResetIB	ResetDB	RSA	TSTP1	TSTP0
49h	DVIP	DVIL	TV	DACPD3	DACPD2	DACPD1	DACPD0	FPD
4Ah	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
4Bh	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0