CH700X Registers Read/Write Operation

This Application Note applies to CH7002, CH7003, CH7004 CH7005, CH7006, CH7007, CH7008 and CH7013, which are denoted as CH700X through out this document.

Regarding CH7009 family encoders register read/write operation, please see AN-41.

Introduction

The CH700X contains a serial port, through which the control registers can be written and read. This port has a two-wire serial interface, Pins SD (bidirectional) - Serial port Data, and SC - Serial port Clock.

The serial port clock line (SC) is input only and is driven by the output buffer of the graphics controller device, which is the clock master in the system. The serial port data line (SD) is either input to or output from CH700X depending on the write or read status. The data on the line can be transferred up to 400 kbit/s. **Figure 1** shows the connection of the serial port interface of CH700X.

Please note that we DO NOT recommend sharing of this serial port with other serial port programmable devices.

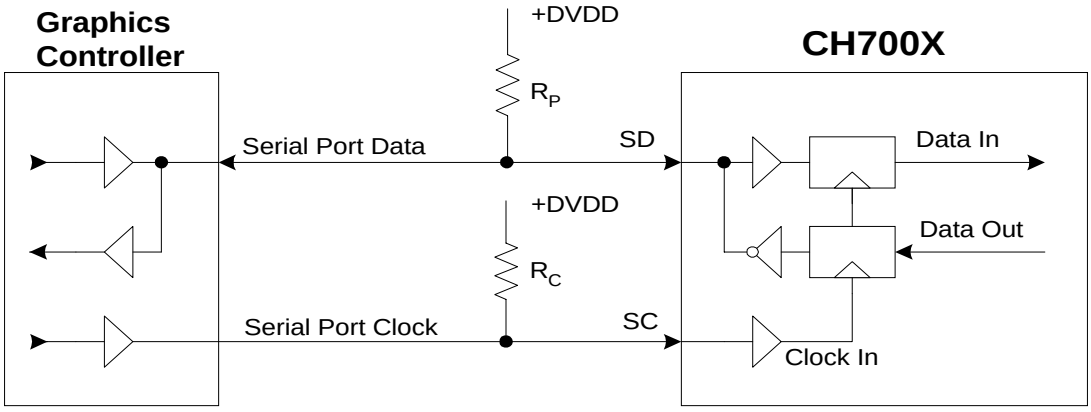


Figure 1: The Connection of the Serial Port Interface of CH700X

Serial Port Operation

Electrical Characteristics for the Serial Port

The electrical specifications of the serial port inputs and outputs are shown in **Figure 1**. A pull-up resistor (R_P) must be connected to a 3.3V ± 10% supply. The CH700X is a device with input levels related to DVDD2.

A weak pull-up resister (R_C) may be added to the clock line to ensure that it is pulled high when the line is free.

Maximum and minimum values of pull-up resistor (R_P)

The value of R_P depends on the following parameters:

- Supply voltage
- Line capacitance
- Number of devices connected (input current + leakage current = I_{input})

The supply voltage limits the minimum value of resistor R_P due to the specified minimum sink current of 2mA at VOL_{max} = 0.4 V for the output stages:

$$R_P >= (V_{DD} - 0.4) / 2 \quad (R_P \text{ in } k\Omega)$$

The line capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of R_P due to the specified rise time. The equation for R_P is shown below:

$$R_P <= 10^3/C \quad \text{(where: } R_P \text{ is in } k\Omega \text{ and C, the total capacitance, is in pF)}$$

The maximum HIGH level input current of each input/output connection has a specified maximum value of 10 µA. Due to the desired noise margin of $0.2V_{DD}$ for the HIGH level, this input current limits the maximum value of R_P. The R_P limit depends on V_{DD} and is shown below:

$$R_P <= (100 \times V_{DD})/ I_{input} \quad \text{(where: } R_P \text{ is in } k\Omega \text{ and } I_{input} \text{ is in } \mu A)$$

Transfer Protocol

Both read and write cycles can be executed in “Auto-increment”, “Single-step” or “Alternating” modes. Auto-increment mode allows you to establish the initial register location, then automatically increments the register address after each subsequent data access (i.e., transfers will be address, data...). The Single-step mode, as a matter of fact, is the Auto-increment mode with a single set of data sending/receiving to/from a specific register. Alternating mode expects a register address prior to each read or write from that locations (i.e., transfers alternate between address and data). A basic serial port transfer protocol is shown in **Figure 2** and is described below.

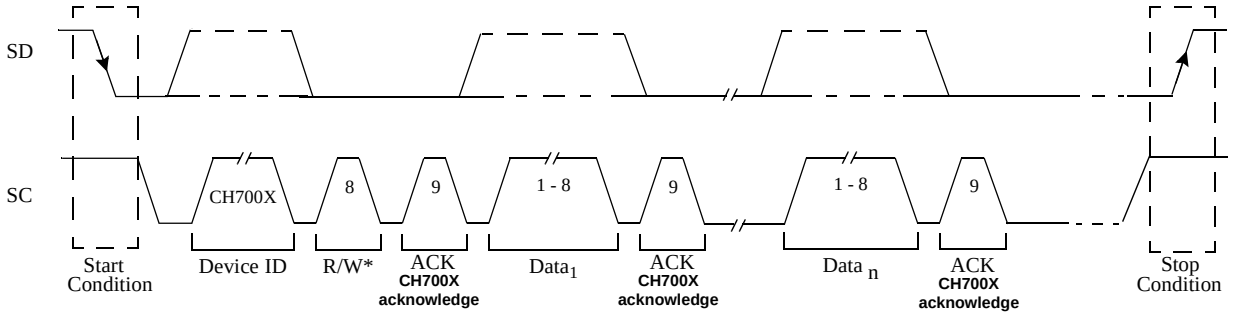


Figure 2: Serial Port Transfer Protocol

Transfer Protocols *(continued)*

1. The transfer sequence is initiated when a high-to-low transition of SD occurs while SC is high; this is the "START" condition. Transitions of address and data bits can only occur while SC is low.
2. The transfer sequence is terminated when a low-to-high transition of SD occurs while SC is high; this is the "STOP" condition.
3. Upon receiving the first START condition, the CH700X expects a Device Address Byte (DAB) from the master device. The value of the device address is shown in the DAB data format below (EAh or EBh).
4. After the DAB is received, the CH700X expects a Register Address Byte (RAB) from the master. The format of the RAB is shown in the RAB data format below (note that B7 is not used).

Device Address Byte (DAB)

B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	0	1	0	1	R/W

R/W Read/Write Indicator

"0": master device will write to the CH700X at the register location specified by the address AR[5:0]

"1": master device will read from the CH700X at the register location specified by the address AR[5:0].

Register Address Byte (RAB)

B7	B6	B5	B4	B3	B2	B1	B0
1	AutoInc	AR[5]	AR[4]	AR[3]	AR[2]	AR[1]	AR[0]

AR[5:0] Specifies the Address of the Register to be Accessed.

This register address is loaded into the Address Register of the CH700X. The R/W access, which follows, is directed to the register specified by the content stored in the Address Register.

AutoInc Register Address Auto-Increment - to facilitate sequential R/W of registers.

"1": Auto-Increment enabled (Auto-increment and Single-step modes).

Write: After writing data into a register, the Address Register will automatically be incremented by one.

Read: Before loading data from a register to the on-chip temporary register (getting ready to be serially read), the Address Register will automatically be incremented by one. However, for the first read after an RAB, the Address Register will not be changed.

"0": Auto-Increment disabled (Alternating mode).

Write: After writing data into a register, the Address Register will remain unchanged until a new RAB is written.

Read: Before loading data from a register to the on-chip temporary register (getting ready to be serially read), the Address Register will remain unchanged.

CH700X Write Cycle Protocols (R/W = 0)

Data transfer with acknowledge is required. The acknowledge-related clock pulse is generated by the master-transmitter. The master-transmitter releases the SD line (HIGH) during the acknowledge clock pulse. The slave-receiver must pull down the SD line, during the acknowledge clock pulse, so that it remains stable LOW during the HIGH period of the clock pulse. The CH700X always acknowledges for writes (see **Figure 3**). Note that the resultant state on SD is the wired-AND of data outputs from the transmitter and receiver.

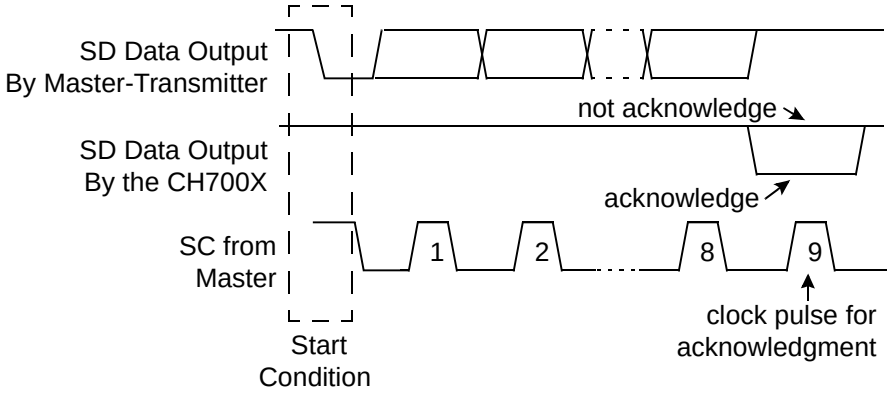
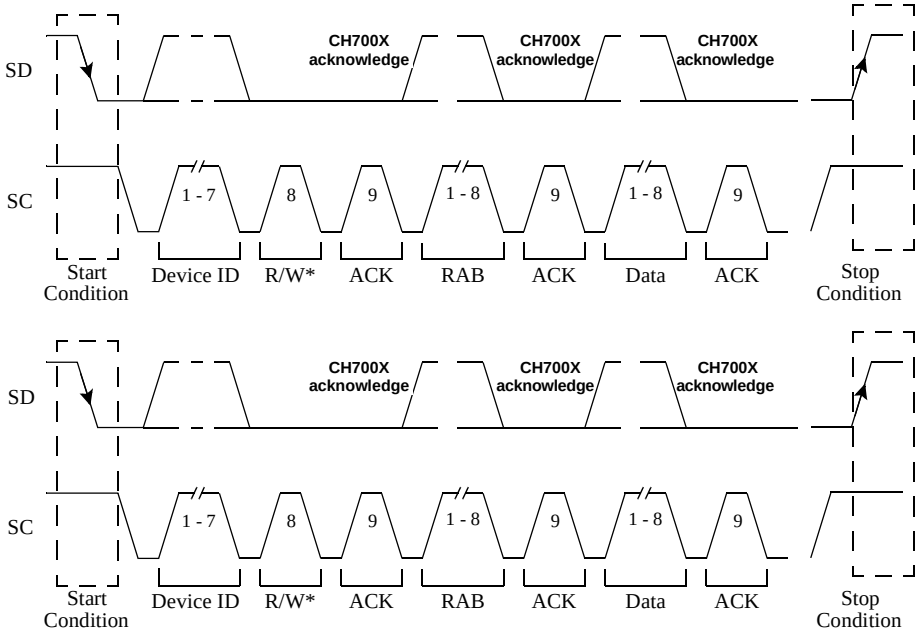


Figure 3: Acknowledge on the Line

- Auto-increment / Single-step modes (AutoInc = 1)

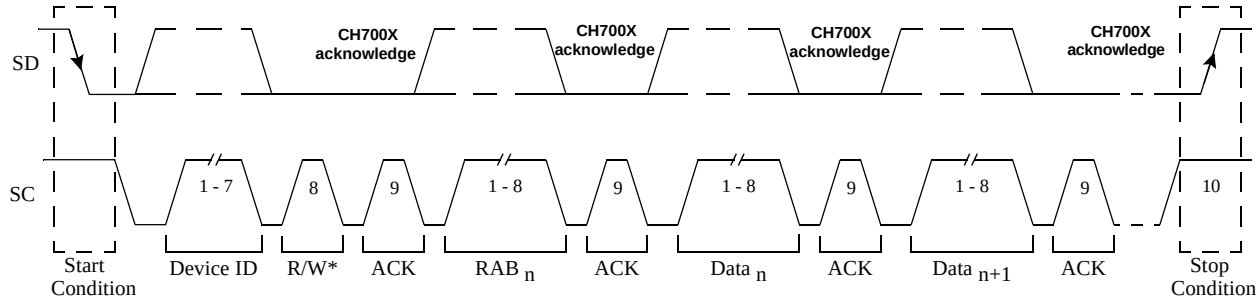
Figure 4 shows two consecutive Single step write cycles. The byte of information, following the Register Address Byte (RAB), is the data to be written into the register specified by AR[5:0] and the lines go to "Stop Condition" immediately after the acknowledgment is received. The cyle is them repeated and so on.



Note: The acknowledge is from the CH700X (slave).

Figure 4: Single-step Write Cycles (2 cycles)

An Auto-increment write cycle is shown in **Figure 5**. During the Auto-increment mode transfers, the register address pointer continues to increment for each data write cycle until AR[5:0] = 3F. The next byte of information represents a new auto-sequencing "Starting address", which is the address of the register to receive the next byte. The auto-sequencing then resumes based on this new "Starting address". The Auto-increment sequence can be terminated any time by either a "STOP" or "RESTART" condition. The write operation can be terminated with a "STOP" condition.

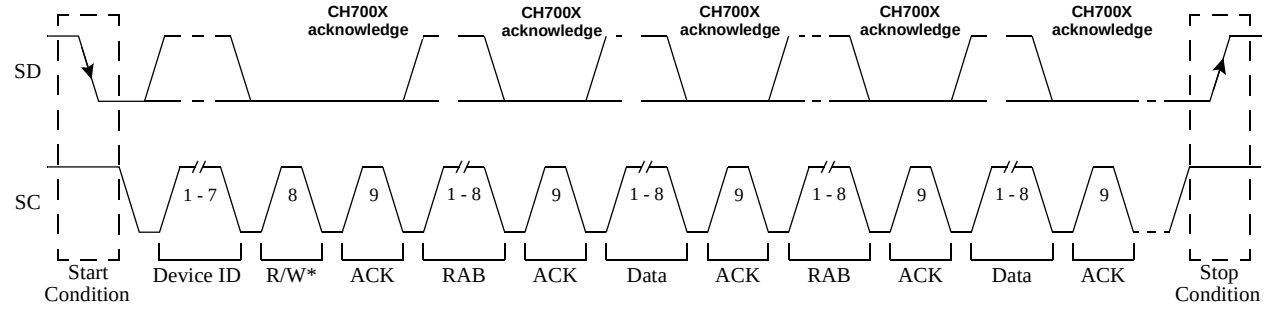


Note: The acknowledge is from the CH700X (slave).

Figure 5: Auto-Increment Write Cycle

- Alternating mode (AutoInc = 0)

Figure 6 shows two consecutive alternating write cycles (AutoInc = 0 and R/W = 0). The byte following the Register Address Byte (RAB), is the data to be written into the register specified by AR [5:0]. And then another RAB is expected from the master device, followed by another data byte, and so on.



Note: The acknowledge is from the CH700X (slave).

Figure 6: Alternating Write Cycles

CH700X Read Cycle Protocols (R/W = 1)

If a master-receiver is involved in a transfer, it must signal the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter CH7003/7004/7005/7006/7007/008 releases the data line to allow the master to generate the STOP condition or the RESTART condition.

- **Auto-Increment / Single modes (AutoInc = 1)**

To read the content of the registers, the master device starts by issuing a "START" condition (or a "RESTART" condition). The first byte of data, after the START condition, is a DAB with R/W = 0. The second byte is the RAB with AR[5:0], containing the address of the register that the master device intends to read from in AR[5:0]. The master device should then issue a "RESTART" condition ("RESTART" = "START", without a previous "STOP" condition). The first byte of data, after this RESTART condition, is another DAB with R/W=1, indicating the master's intention to read data hereafter. The master then reads the next byte of data (the content of the register specified in the RAB). For Single-step mode, a "Stop" condition or "Restart" condition is sent out immediately after the acknowledge of data read (see **Figure 7**).

Transfer Protocols *(continued)*

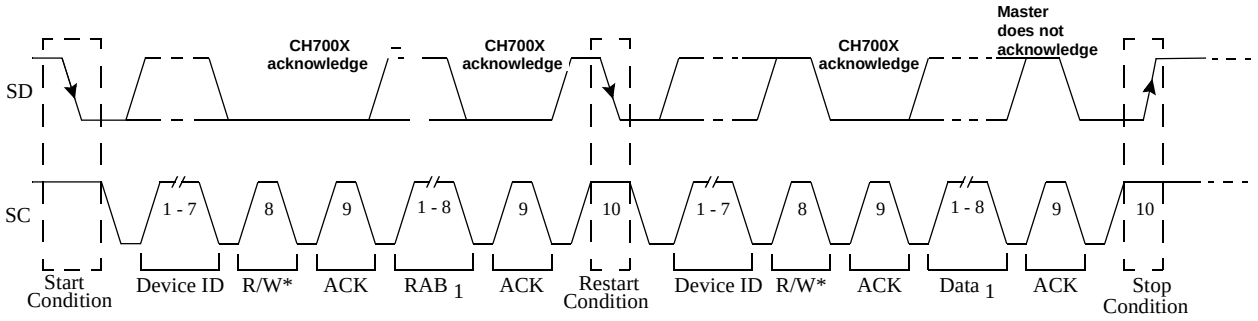


Figure 7: Single-step Read Cycle

For Auto-increment read cycle, the address register will be incremented automatically and subsequent data bytes can be read from successive registers without providing a second RAB.

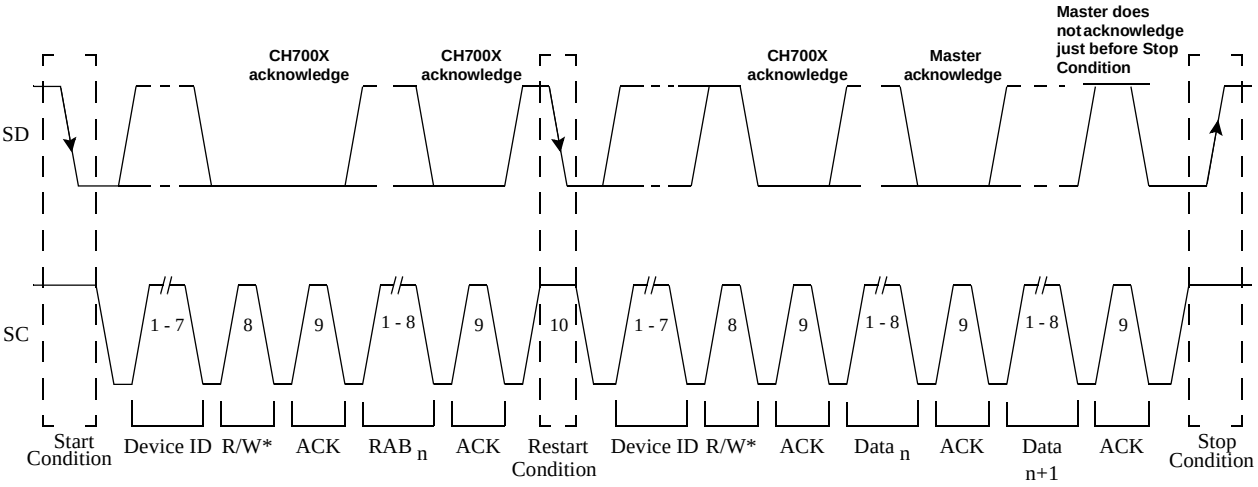


Figure 8: Auto-increment Read Cycle

Regarding the Auto-increment mode, the address register continues to increment for each read cycle. When the content of the address register reaches 2Ah, it will wrap around and start from 00h again. The auto increment sequence can be terminated by either a “STOP” or “RESTART” condition. The read operation can be terminated with a “STOP” condition. **Figure 8** shows an Auto-increment read cycle terminated by a STOP condition.

- Alternating mode (AutoInc = 0)

In Alternating mode, another RESTART condition, followed by another DAB with R/W = 0 and RAB, is expected from the master device. The master device then issues another RESTART, followed by another DAB. After that, the master may read anotehr data byte, and so on. In summary, a RESTART condition, followed by a DAB, must be produced by the master before each of the RAB, and before each of the data read events. Two consecutive alternating read cycles are shown in **Figure 9**.

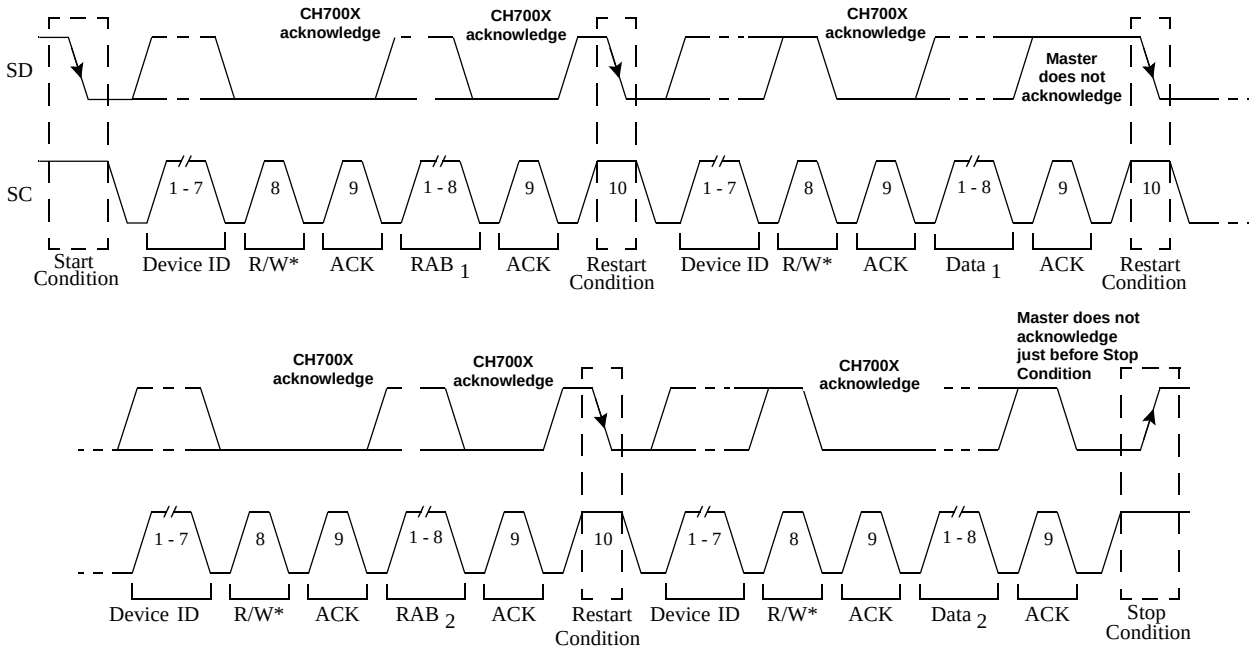


Figure 9: Alternating Read Cycle

Registers Map of CH700X

Table 1 shows the non-Macrovision registers map of CH700X.

Table 1: CH700X non-Macrovision Registers Map

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00H	IR2	IR1	IRO	VOS1	VOS0	SR2	SR1	SR0
01H			FC1	FC0	FY1	FY0	FT1	FT0
02H								
03H	FLFF	CVBW	CBW1	CBW0	YPEAK	YSV1	YSV0	YCV
04H		DACG	Reserved		IDF3	IDF2	IDF1	IDF0
05H								
06H	CFRB	M/S*	Reserved	MCP	XCM1	XCM0	PCM1	PCM0
07H	SAV7	SAV6	SAV5	SAV4	SAV3	SAV2	SAV1	SAV0
08H						SAV8	HP8	VP8
09H	BL7	BL6	BL5	BL4	BL3	BL2	BL1	BL0
0AH	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
0BH	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
0CH								
0DH					DES	SYO	VSP	HSP
0EH				SCART	Reset*	PD2	PD1	PD0
0FH								
10H					YT	CT	CVBST	SENSE
11H						CE2	CE1	CE0
12H								
13H				Reserved	Reserved	N9	N8	M8
14H	M7	M6	M5	M4	M3	M2	M1	M0
15H	N7	N6	N5	N4	N3	N2	N1	N0
16H								
17H			SHF2	SHF1	SHF0	SCO2	SCO1	SCO0
18H					FSCI31	FSCI30	FSCI29	FSCI28
19H					FSCI27	FSCI26	FSCI25	FSCI24
1AH					FSCI23	FSCI22	FSCI21	FSCI20
1BH	GPIOIN1	GPIOIN0	DVDD2	P-OUTP	FSCI19	FSCl18	FSCl17	FSCl16
1CH	GOENB1	GOENB0	DSM	DSEN	FSCI15	FSCl14	FSCl13	FSCI12
1DH					FSCI11	FSCl10	FSCl9	FSCI8
1EH					FSCI7	FSCI6	FSCI5	FSCI4
1FH					FSCI3	FSCI2	FSCI1	FSCI0
20H			PLLCPl	PLLCAP	PLLS	PLL5VD	PLL5VA	MEM5V
21H				CIV25	CIV24	ClVH1	ClVH0	AClV
22H	CIV23	CIV22	CIV21	CIV20	CIV19	CIV18	CIV17	CIV16
23H	CIV15	CIV14	CIV13	CIV12	CIV11	CIV10	CIV9	CIV8
24H	CIV7	CIV6	CIV5	CIV4	CIV3	CIV2	CIV1	CIVO
25H	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
26H	TS3	TS2	TS1	TS0	RSA	BST	NST	TE
27H			MS2	MS1	MSO	MTD	YLM8	CLM8
28H	YLM7	YLM6	YLM5	YLM4	YLM3	YLM2	YLM1	YLM0
29H	CLM7	CLM6	CLM5	CLM4	CLM3	CLM2	CLM1	CLM0
3FH	Reserved	Reserved	AR5	AR4	AR3	AR2	AR1	AR0