Design Tips To CH7009/7010/7301 DVI Display at 1600 x 1200 Resolution

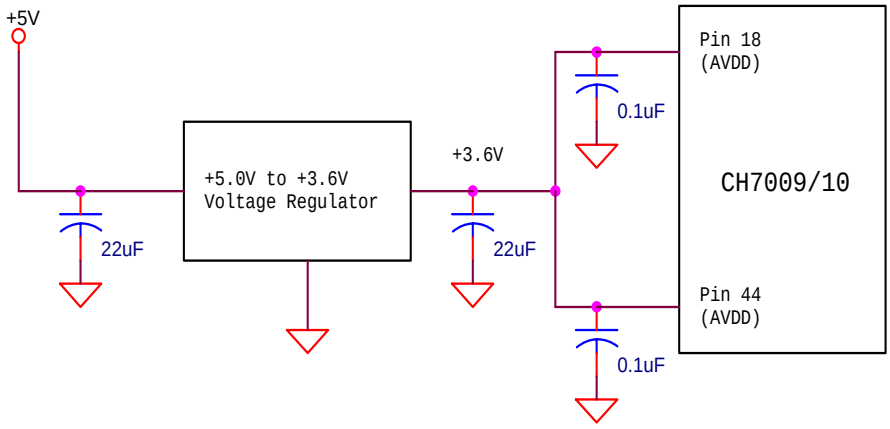
Introduction

This application note focuses on the design awareness to CH7009/7010/7301 DVI display at 1600 x 1200 resolution. The guidelines discussed here are intended to optimize the applications for this product operating at frequencies as high as 162 MHz. Designers are urged to implement the configurations and evaluate the performance of the system prior to bringing the design to production.

The CH7009/7010/7301 PLL supply voltage comes from AVDD (pins 18 & 44), which may accept +3.3V ~ +3.6V power input. When AVDD pins are given +3.3V while operating at 1600 x 1200 resolution with 60 Hz refresh rate (pixel clock = 162MHz), jitters may be seen from the DVI display. The jitters are due to the unstable PLL within CH7009/7010/7301. In order to optimize PLL circuitry, the following design tips should be implemented.

- **Hardware**

When operating CH7009/7010/7301 for DVI display at 1600 x 1200 resolution, we recommend that the AVDD input voltage be set at +3.6V in order to guarantee PLL to lock. A +5.0V to +3.6V voltage regulator can be used as an example shown below:



- **Register Settings**

In addition to the PLL supply voltage, some software register settings should be followed for the best DVI display at various frequency range. The optimal register values are listed in the table below:

Register Settings For Various Frequency Ranges				
Registers		50MHz +/- 25MHz	100MHz +/- 25MHz	140MHz +/- 25MHz
31h	TCTL	0x00	0x00	0x00
32h	TVCO	0x23	0x23	0x2D
33h	TPCP	0x08	0x04	0x07
34h	TPD	0x16	0x26	0x26
35h	TPVT	0x30	0x30	0x30
36h	TPF	0x60	0x60	0xE0
37h	TVCOO	0x00	0x00	0x00