

Description of Operation

The stability of LVDS PLL should be established before enabling frequency spreading. It is suggested that the following register settings in **Table 1** be followed.

Table 1: LVDS PLL Registers Settings for Spread Spectrum Operation

Register Symbol	Register/bits	Parameter	Settings	Explanations
LVCTL7	7Dh[4:2]	SS mode	110	Internal Mode Enabled, External Mode Disabled
OUTEN	73h[2:0]	CP Current	110	Charge pump current = 23uA
LPDLFR	76h[6:4]	LP resistor	010	Rloop = 1000ohm
LVCTL2	78h[6:5]	LP capacitor	00	Cloop = 100pF
LPVC	72h[3:0]	VCO unit	1100	VCO gain = 3.3unit
LPSSC	75h[2:0]	I ramp	100	I ramp = 40uA
-----	N/A	PLLCAP	0.1nF	Connected externally on board

The magnitude of the frequency spreading can be increased by increasing the Spread Spectrum coupling capacitor C_{ss}. The value of C_{ss} is controlled by Reg 75h[6:3]. **Table 2** shows the details of the spread spectrum values.

Table 2: Spread Spectrum Values Set by C_{ss}

Input f (MHz)	SS +/- 1.5%		SS +/-2.5%	
	Delta f (MHz)	75h[6:3]	Delta f (MHz)	75h[6:3]
31.500	0.95	1000	1.58	1100
35.500	1.07	1000	1.78	1100
36.000	1.08	1000	1.80	1100
40.000	1.20	0100	2.25	0010
43.163	1.30	0100	2.16	0010
45.000	1.35	0100	2.25	0010
48.000	1.44	1100	2.40	1010
65.000	1.95	0010	3.25	1101
99.000	1.49	1100	2.48	1010
108.000	1.62	1100	2.70	0110
139.050	2.09	0010	3.48	1011
148.500	2.23	0010	3.71	1011
152.000	2.28	0010	3.80	0111
162.000	2.43	1010	4.05	0111