A PCB Design Guideline to Prevent DVI Signaling Power Interference in the CH7009 Family Chips Applications

1. Introduction

This application note focuses on a special PCB design care for the CH7009 family (CH7009/CH7010/CH7301) DVI applications. Its main purpose is to attack a power-interference problem ignited by CH7009 DVI power pin, of which the power is fed by DVI panel signals through the DVI cable connecting to CH7009. The PCB designers are strongly suggested that this design guideline be followed to prevent this power interference problem which may occasionally cause system boot-up or system power-down sequence disorder.

2. Explanation to the Problem

The DVI power pins (pins 23, 29 TVDD) of CH7009 family may be fed by the DVI panel signals with a certain level of voltage when the system (containing CH7009) is powered off and DVI panel is powered on. This is because that CH7009 as well as all ICs have input diode protection - one to ground and one to VDD, and the power is fed back to the TVDD power pins through this protection diode.

3. Solutions to the Problem

The way to prevent the power interference is to isolate the CH7009 chip TVDD power supply with a voltage regulator or a simple low forward-voltage diode. Putting a low forward-voltage diode (See **Figures 1**, **2**) between 3.3V power input and TVDD (pins 23, 29) of CH7009 solves the problem with a sacrifice of minor voltage drop to TVDD. A better way to the solution is to isolate CH7009 power from other chips on board by using a dedicated voltage regulator for the CH7009 family chip (See **Figures 3**).

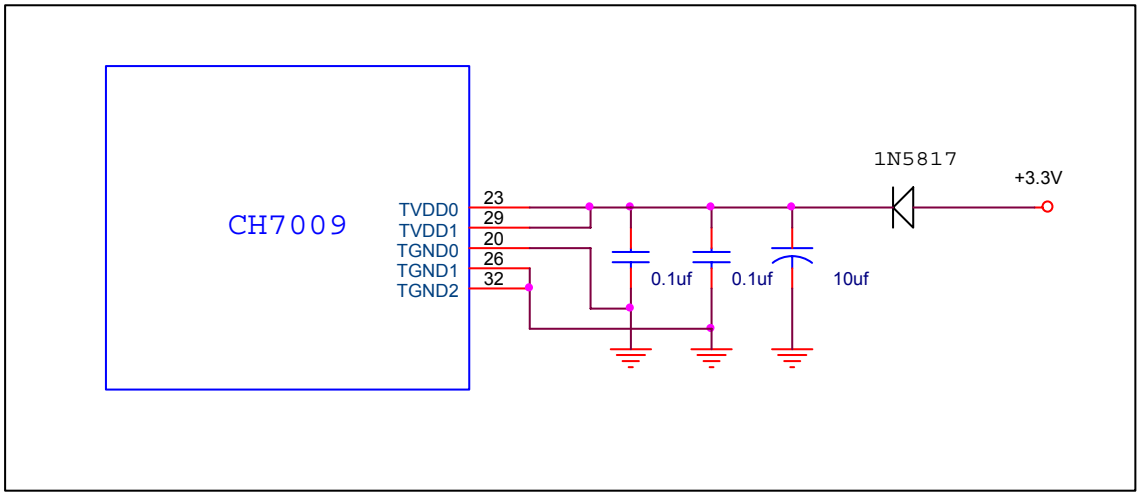

Figure 1: Isolate the CH7009 family TVDD power with a low forward-voltage diode (such as 1N5817).

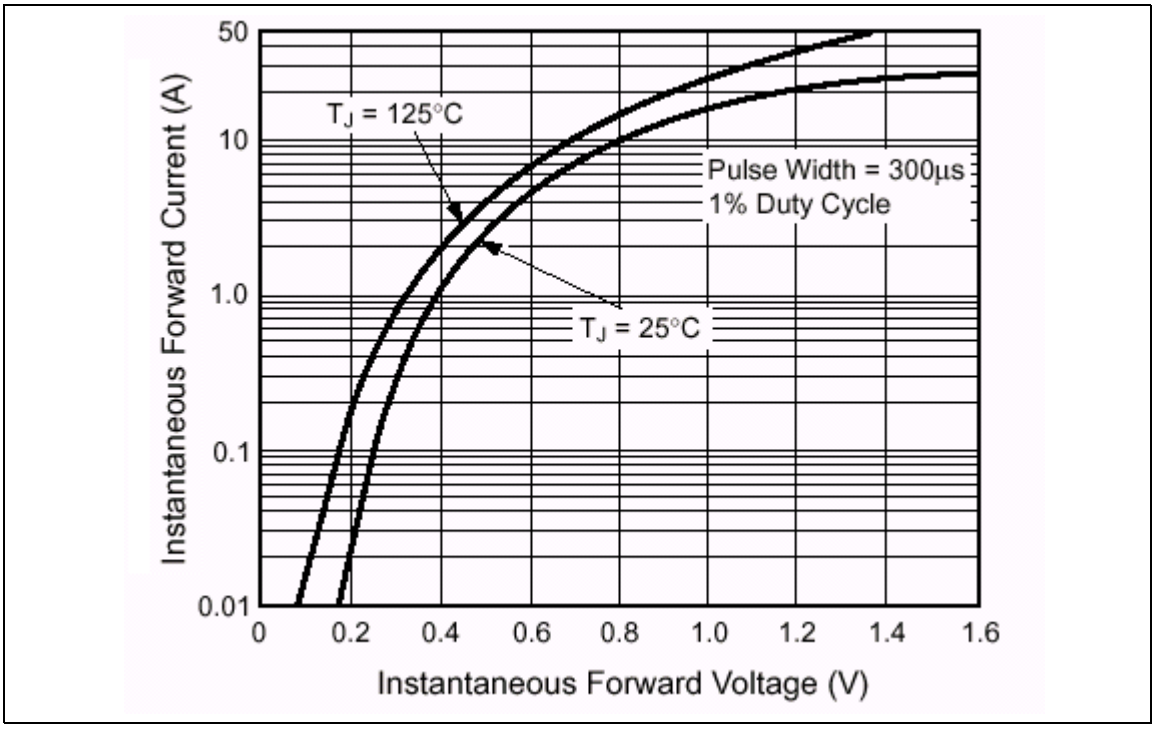

Figure 2: The forward-voltage characteristics of diode 1N5817

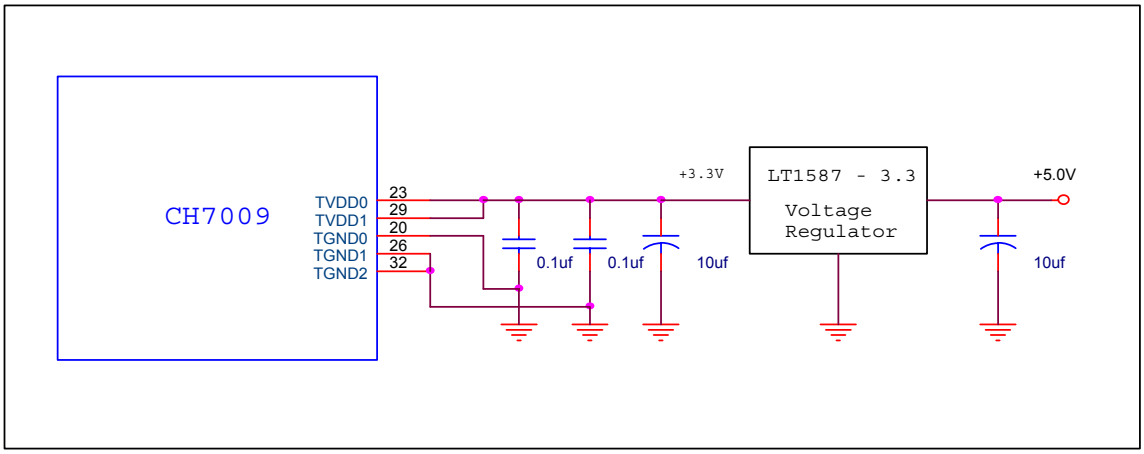

Figure 3: Isolate the CH7009 family TVDD power with a 5.0V - 3.3V voltage regulator (such as LT1587-3.3)

4. Chip Performance with the Solutions Implemented

Figures 4 – 7 show the eye-diagrams of the CH7009 family chips DVI outputs. Both of the above solutions have been tested and showed that they are robust solutions. Please note that when low forward-voltage diode solution is used, the diode voltage drop should be as small as possible so that the TVDD voltage remains above 3.0V.

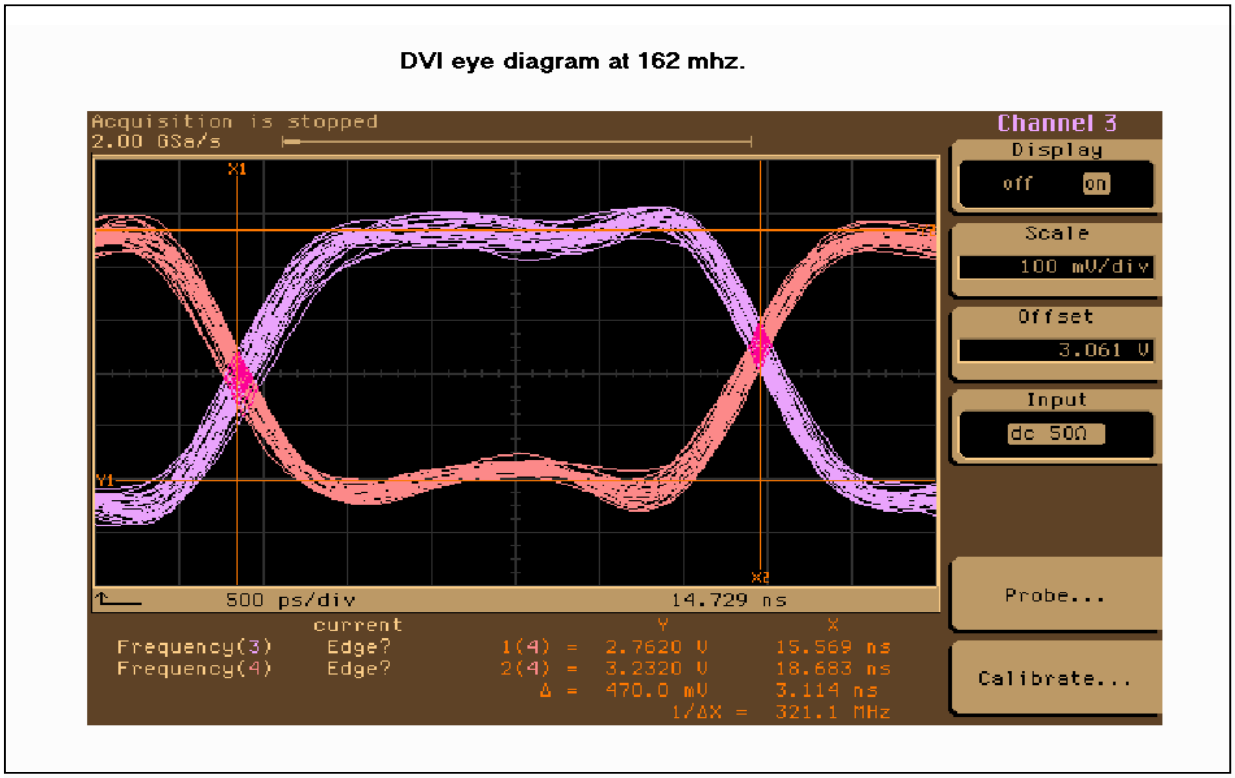

Figure 4: DVI Eye-diagram at 162 MHz (1600 x 1200 pixels) -1

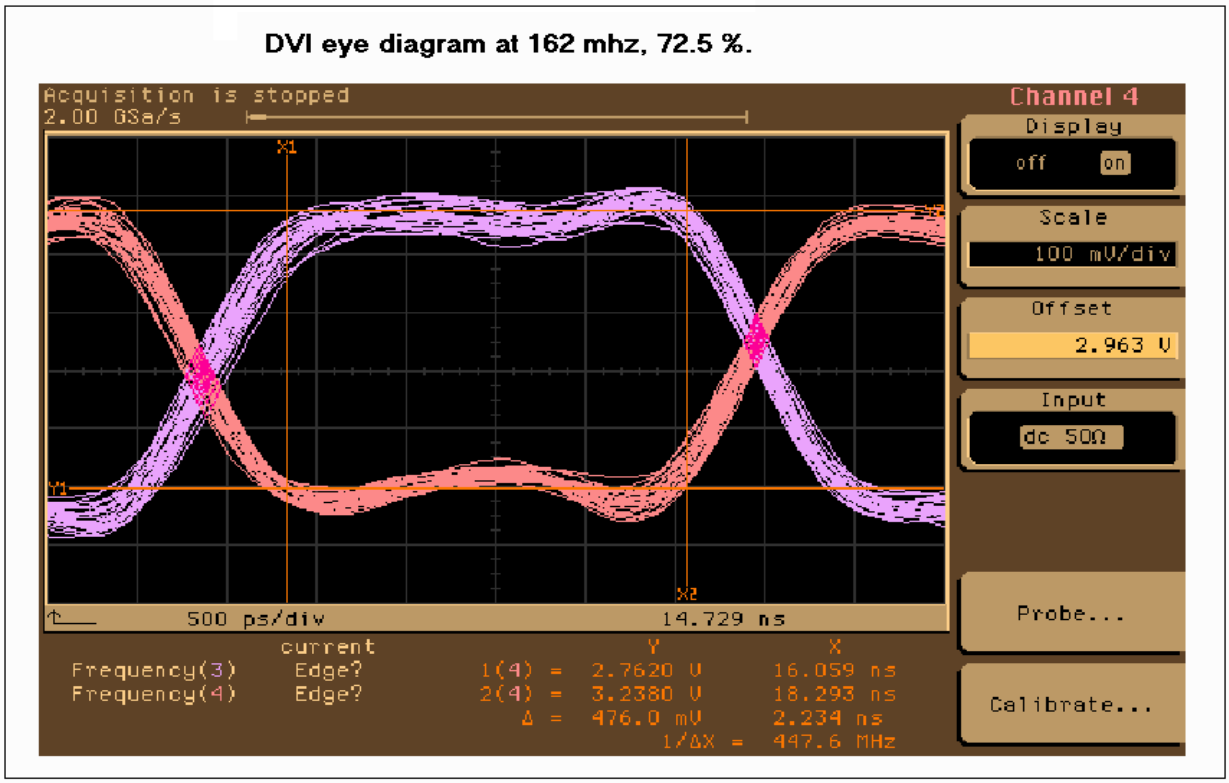

Figure 5: DVI Eye-diagram at 162 MHz (1600 x 1200 pixels) –2

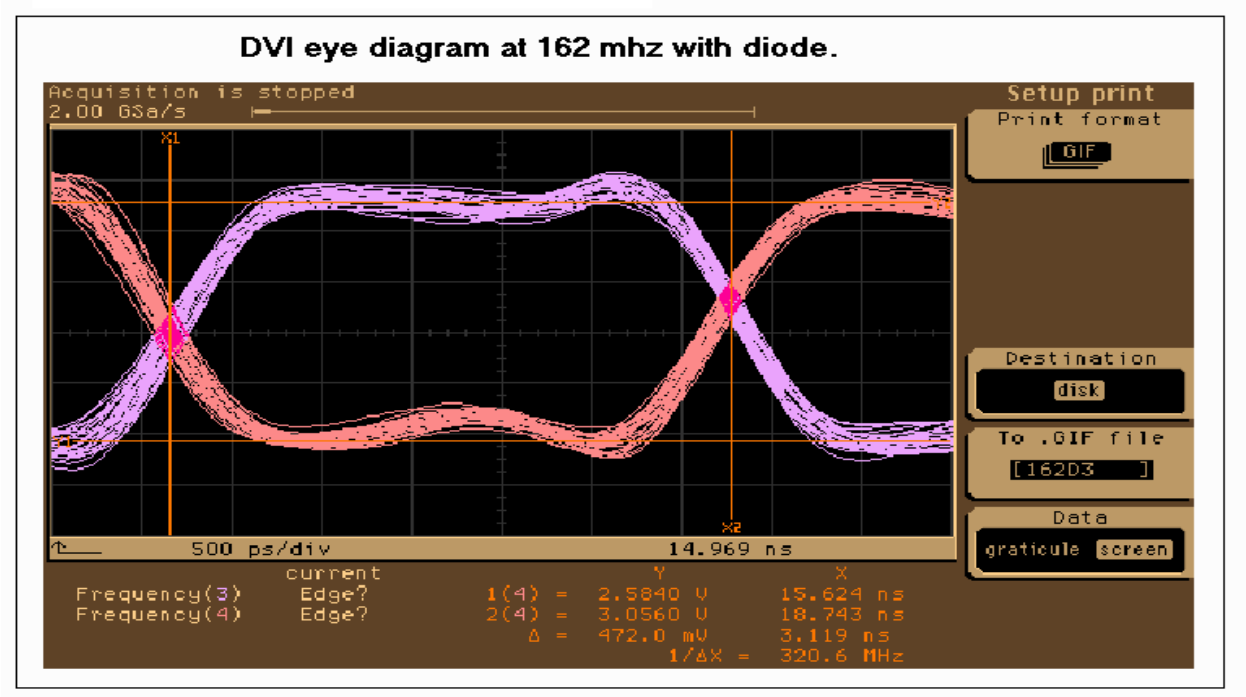

Figure 6: DVI Eye-diagram at 162 MHz (1600 x 1200 pixels, with diode 1N5817) –1

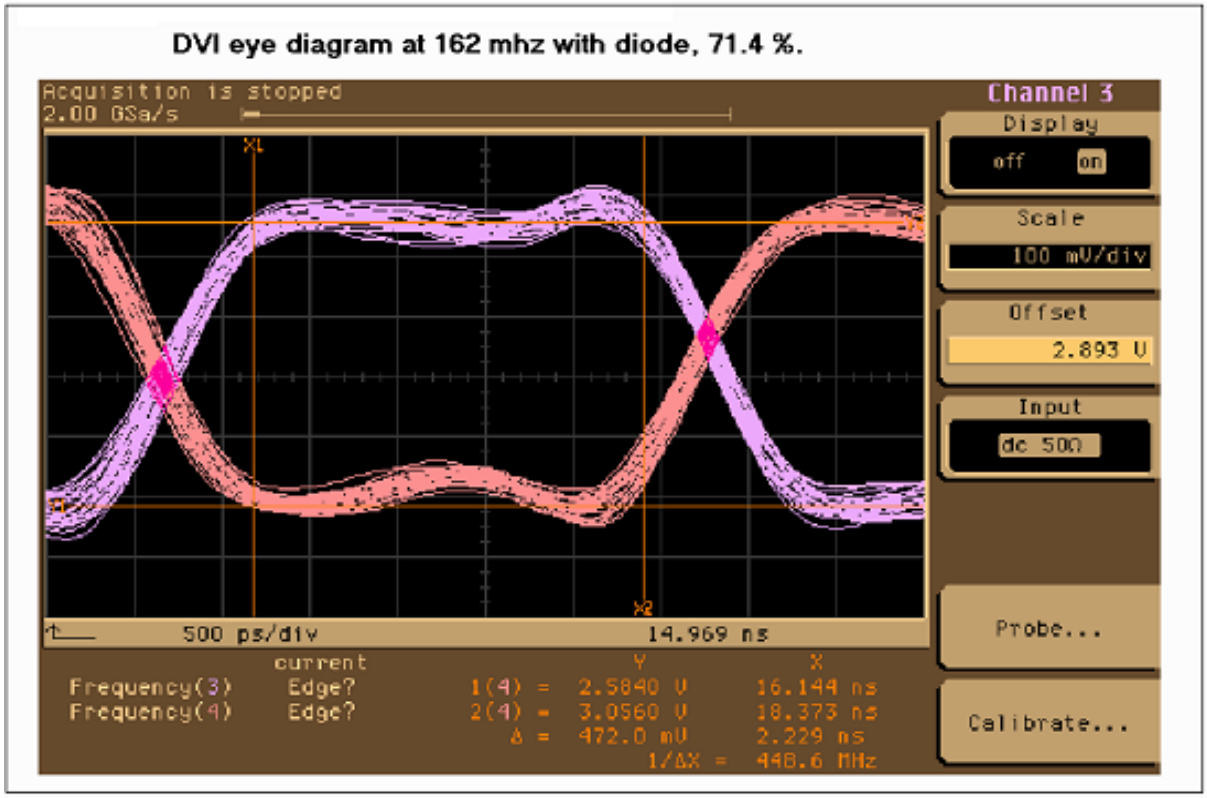

Figure 7: DVI Eye-diagram at 162 MHz (1600 x 1200 pixels, with diode 1N5817) –2

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