CH7xxx SDTV/HDTV Encoder TV Connection Detection

1. Introduction

This application note explains the TV connection detection method for Chrontel CH7xxx SDTV/HDTV Encoders.

2. Video Output

For video to be displayed, the DAC connection detection procedure must first be completed, then afterwards depending on which DACs have sensed a connection, will the Chrontel encoder drive out the corresponding video signals to the connected DACs.

2.1 Connection Detection Procedure

Connection Detect (CD) Register, Register 20h

Bit	7	6	5	4	3	2	1	0
SYMBOL	Reserved	XOSC2	Reserved	DACT3	DACT2	DACT1	DACT0	SENSE
TYPE	R/W	R/W	R/W	R	R	R	R	R/W
DEFAULT:	0	1	0					0

DACT[3:0] (bits 4-1) and SENSE (bit 0) bits of Register CD provide a means to sense the connection of a TV to the four DAC outputs. The status bits, DACT[3:0] correspond to the loading resistance of the four DAC outputs. However, the values contained in these status bits ARE NOT VALID until a sensing procedure is performed. Use of this Register requires a sequence of events to enable the sensing of outputs, then reading out the applicable status bits.

The connection detection procedure is as follows:

1. Enable all DACs by setting the Power Management Register, Register 49h, accordingly.

2. Set the SENSE bit of the Connection Detect (CD) Register, Register 20h - bit 0 to ’1’. This forces a constant dc current output from the DACs. Note that when SENSE = ’1’, these 4 DACs send out a DC current and no TV synchronization pulses are asserted.

3. Reset the SENSE bit to ’0’. This triggers a comparison between the voltage present on DAC pins itself and the internal reference voltage used for comparison. During this step, each of the four DAC status bits that corresponds to the individual DAC outputs will be set to ’0’ if it is NOT CONNECTED, and ’1’ if it is CONNECTED.

4. Read the status bits. The status bits, DACT[3:0], now contain valid information which can be read to determine which DACs are connected externally. A ’1’ indicates a valid connection and a ’0’ indicates an unconnected DAC.

2.2 Composite and S-Video Output

(A) Composite output can be generated through the DAC associated with CVBS. Only when a load on this pin has been detected and the HDTV bit (if the encoder has HDTV out), Register 14h - bit 0, is set to ’0’, will a composite signal be generated and gated out of this DAC.*

(B) As for s-video, when the DAC associated to the Chroma signal (C) senses a connection and the HDTV bit (if the encoder has HDTV out), Register 14h - bit 0, is set to ’0’, the s-video signals will be gated out of the designated s-video DACs.*

If both **(A)** and **(B)** are fulfilled, Composite and s-video signals will be sent out simultaneously. *

*DACs associated with this desired video output must be powered on.

2.3 HDTV and SDTV Component Video Output

If the encoder chip is capable of driving YPrPb - Component Video, and HDTV Component Video output is desired, the HDTV bit, register 14h - bit 0, must be set to ’1’. If the DAC corresponding to the Pb signal senses a connection, the HDTV YPrPb video signals will be generated and gated out of the corresponding DACs. The default value of the HDTV bit is ’0’. DACs associated with Y, Pr, and Pb must be powered on.

If the encoders are capable of driving YPrPb - SDTV DVD modes 37 and 38 (480i and 576i), and these modes are desired, the HDTV bit should be set to ’0’. If the DAC corresponding to the Pb signal senses a connection, the SDTV DVD video signals will be generated and gated out of the corresponding DACs. DACs associated with Y, Pr, and Pb must be powered on.

2.4 Explanation of TV Flash During Detection Process

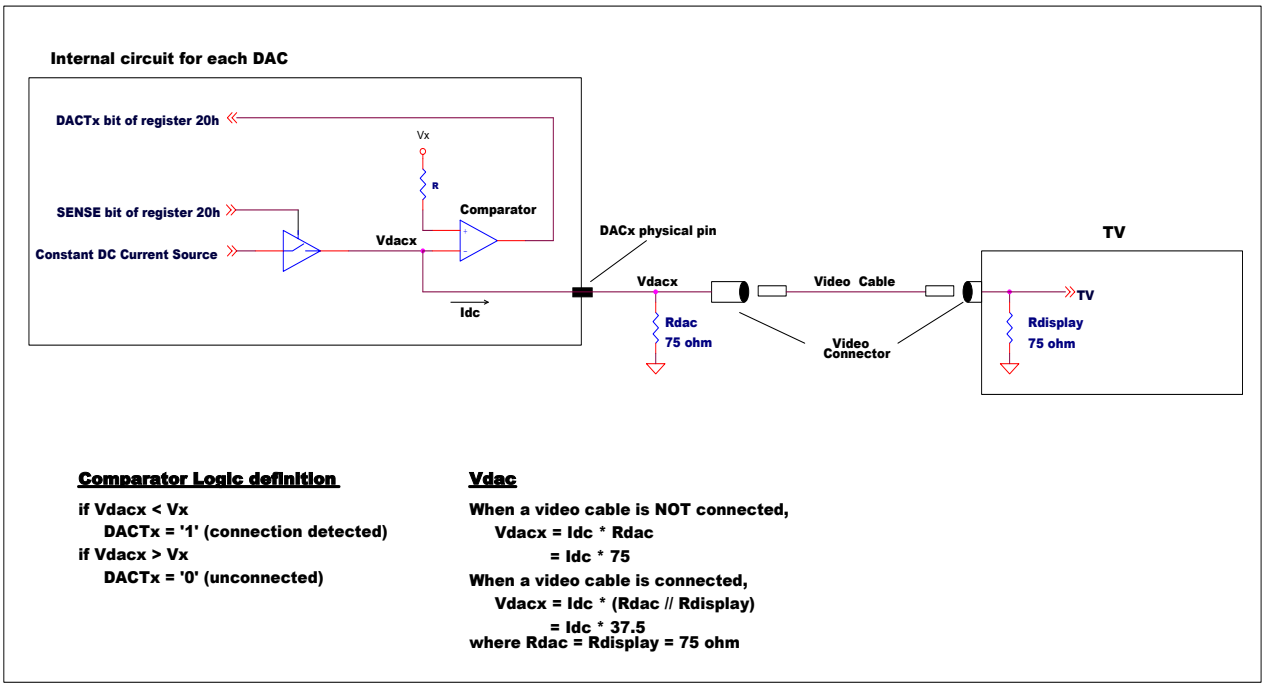

Figure 1: Connection Detection Diagram

Referring to **Figure 1**, it can be seen why the TV flashes during the connection detection process. The flash is due to the small constant DC current that is driven out of the DACs and flows into the connected TV during the connection detection process. This symptom is normal and will not cause damage to the connected TV.

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