CH7017 TV Encoder / LVDS Transmitter

Features

TV-Out:

- VGA to TV conversion supporting up to 1024x768
- Macrovision™ 7.X copy protection support
- Two variable-voltage digital input ports.
- Simultaneous LVDS and TV output.
- TrueScale™ rendering engine supports under-scan in all TV output resolutions †¥
- Enhanced text sharpness and adaptive flicker removal with up to 7 lines of filtering ¥
- Support for all NTSC and PAL TV formats
- Outputs CVBS, S-Video and RGB
- Support for SCART connector
- TV / Monitor connection detect
- Output video switch for easy wiring to connectors

LVDS-Out:

- Single / Dual LVDS transmitter
- Dual LVDS supports pixel rate up to 330Mpixels/sec. when both 12-bit input ports are ganged together.
- Panel fitting scaler – up scale to 1600x1200
- LVDS low jitter PLL accepts spread spectrum input
- LVDS 18-bit and 24-bit output
- 2D dither engine for 18-bit panels
- Panel protection and power down sequencing
- Programmable power management
- Hot Plug detection

- Support for second CRT DAC bypass mode
- Four 10-bit video DAC outputs
- Fully programmable through serial port
- Complete Windows and DOS driver support
- Variable voltage interface to graphics device
- Offered in a 128-pin BGA and LQFP package

1.0 General Description

The CH7017 is a Display Controller device which accepts two digital graphics input data streams. One data stream outputs through an LVDS transmitter to an LCD panel, while the other data stream is encoded for NTSC or PAL TV and outputs through a 10-bit high speed DAC. The TV encoder device encodes a graphics signal up to 1024x768 resolution and outputs the video signals according to NTSC or PAL standards. The LVDS transmitter operates at pixel speeds up to 165MHz per link, supporting 1600x1200 panels at 60Hz refresh rate.

The device can also accept one graphics data stream over two 12-bit wide variable voltage ports which support nine different data formats including RGB and YCrCb (RGB must be used for LVDS output). A maximum of 330M pixels per second can be output through dual LVDS links.

The TV-Out processor will perform non-interlaced to interlaced conversion with scaling, flicker filtering, and encoding into any of the NTSC or PAL video standards. The scaler and flicker filter are adaptive and programmable for superior text display. Eight graphics resolutions are supported up to 1024 by 768 with full vertical and horizontal under-scan capability in all modes. A high accuracy low jitter phase locked loop is integrated to create outstanding video quality. Support is provided for Macrovision™. In addition to TV encoder modes, bypass modes are included which allow the TV DAC's to be used as a second CRT DAC.

The LVDS transmitter includes a panel fitting up-scaler and a programmable dither function for support of 18-bit panels. Data is encoded into commonly used formats, including those detailed in the OpenLDI and the SPWG specifications. Serialized data outputs on three to eight differential channels.

† Patent number 5,781,241
¥ Patent number 5,914,753

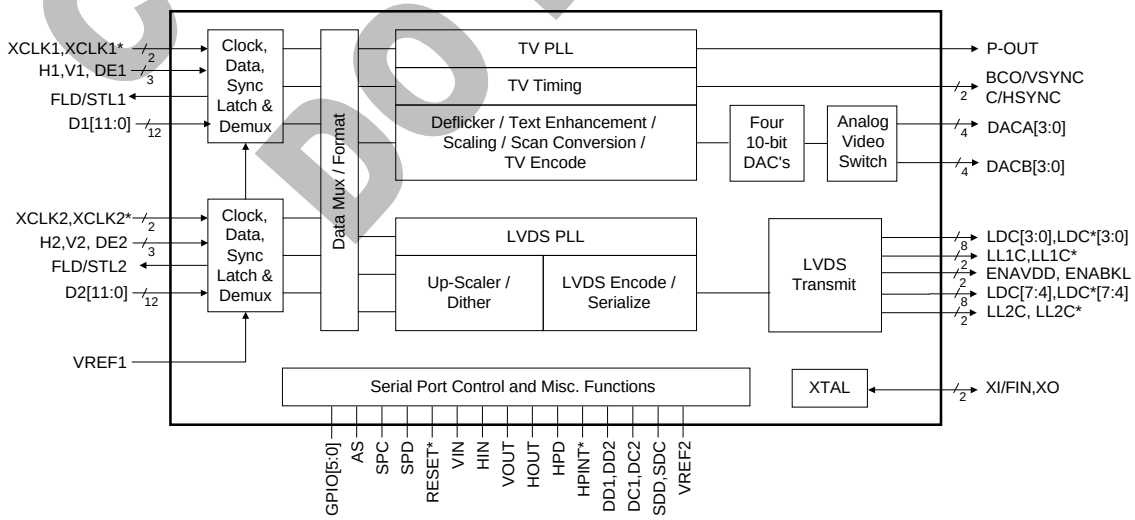

Figure 1: Functional Block Diagram

2.0 Pin Assignment

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2.1 Package Diagram

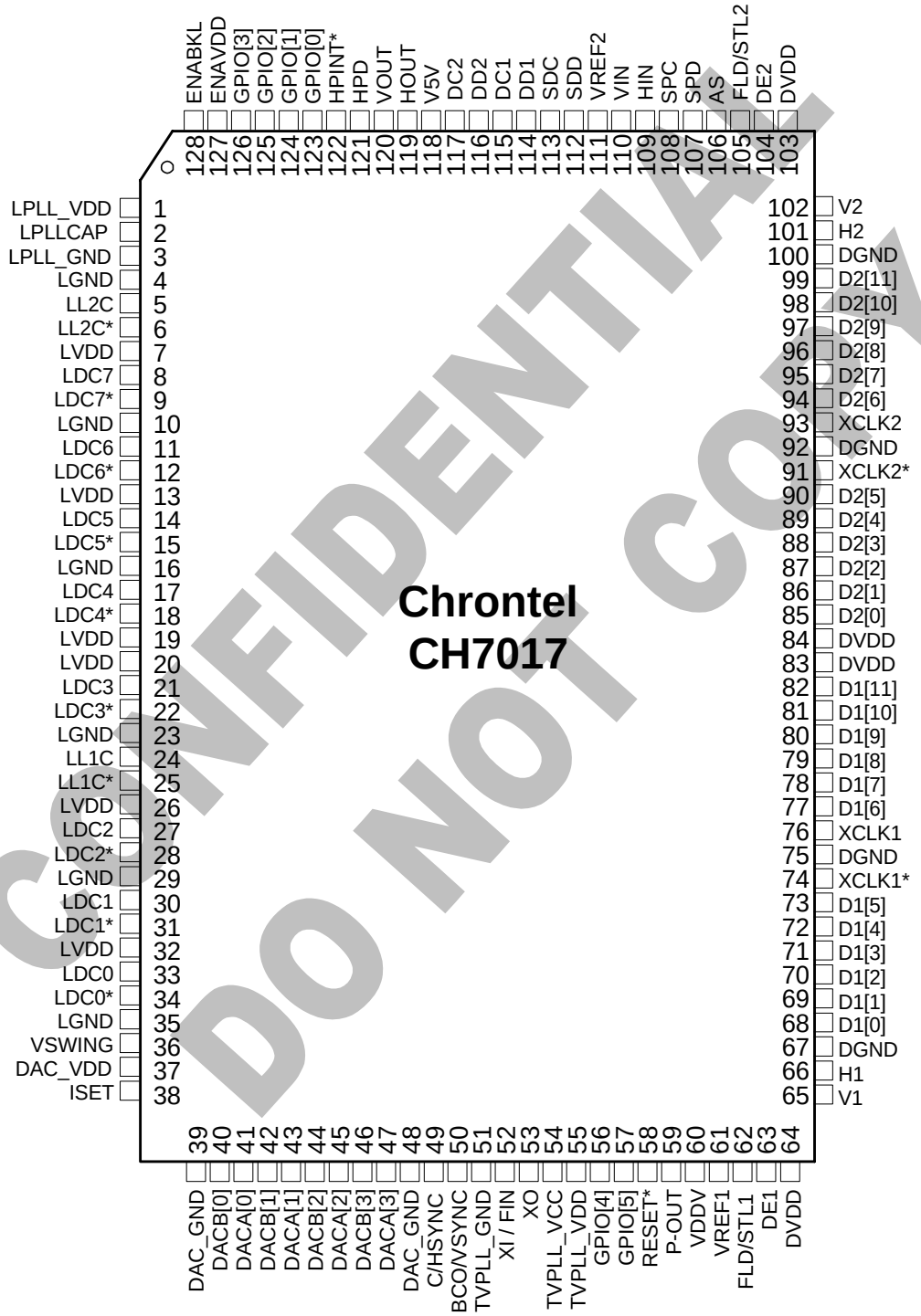

Figure 2: 128 Pin LQFP Package (Top View)

2.2 Pin Description

Table 1: Pin Description

Pin #	# of Pins	Type	Symbol	Description
66, 101	2	In/Out	H1, H2	**Horizontal Sync Input / Output** When the SYO control bit is low, these pins accept a horizontal sync inputs for use with the input data. The amplitude will be 0 to VDDV. VREF1 is the threshold level for these inputs. These pins must be used as inputs in RGB Bypass mode. When the SYO control bit is high, the TV encoder will output a horizontal sync pulse 64 pixels wide to one of these pins. The output is driven from the DVDD supply. This output is valid only when TV-Out is in operation.
65, 102	2	In/Out	V1, V2	**Vertical Sync Input / Output** When the SYO control bit is low, these pins accept a vertical sync inputs for use with the input data. The amplitude will be 0 to VDDV. VREF1 signal is the threshold level. These pins must be used as inputs in RGB Bypass mode. When the SYO control bit is high, the TV encoder will output a vertical sync pulse one line wide to one of these pins. The output is driven from the DVDD supply. This output is valid only when TV-Out is in operation.
63, 104	2	In	DE1, DE2	**Data Enable** These pins accept a data enable signal which is high when active video data is input to the device, and remains low during all other times. The levels are 0 to VDDV. VREF1 is the threshold level. One of these inputs is used by the LVDS links. The TV-Out function uses H and V sync signals and values in the SAV register as reference to active video.
62, 105	2	Out	FLD/STL1, FLD/STL2	**TV Field / Flat Panel Stall Signal** These outputs can be programmed to be either a TV Field output from the TV encoder or a Stall output from the flat panel Up-scaler. These outputs are tri-stated upon power up.
107	1	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port, and uses VREF2 / 2 as the threshold voltage. Divide by 2 function is generated on-chip.
108	1	In	SPC	**Serial Port Clock Input** This pin functions as the clock input of the serial port, and uses VREF2/2 as the threshold voltage. Divide by 2 is generated on-chip
106	1	In	AS	**Address Select** (Internal Pull-up) This pin determines the device address of the serial port (TBD).
112	1	In/Out	SDD	**Low-Voltage DDC Serial Data** Low-voltage serial data for DDC. VREF2 is used to generate internal bias voltage for the level shifter.
113	1	In/Out	SDC	**Low-Voltage DDC Serial Clock** Low-voltage serial clock for DDC. VREF2 is used to generate internal bias voltage for the level shifter.
114, 116	2	In/Out	DD1, DD2	**DDC Serial Data** Serial data for DDC. (0V to 5V)
111	1	In	VREF2	**Reference Voltage 2** Bias Voltage for SDD, SDC, SPD and SPC port. This voltage equals to the maximum voltage seen by the ports. (1.5V to 3.3V).
115, 117	2	In/Out	DC1, DC2	**DDC Serial Clock** Clock for DDC. (0V to 5V)
123-126, 56, 57	6	In/Out	GPIO[5:0]	**General Purpose Input / Output [5:0]** (Internal Pull-up) These pins provide general purpose I/O and are controlled via the serial port. (3.3V)
127	1	Out	ENAVDD	**Panel Power Enable** Enable panel VDD. (3.3V)
128	1	Out	ENABLK	**Back Light Enable** Enable Back Light of LCD Panel. (3.3V)

Table 1: Pin Description (Continue)

Pin #	# of Pins	Type	Symbol	Description
121	1	In	HPD	**Hot Plug Detect** (Internal Pull-down This input pin determines whether a CRT monitor is connected to the VGA connector. When terminated, the monitor is required to apply a voltage greater than 2.4 volts. Changes on the status of this pin will be relayed to the graphics controller via the HPINT* pin pulling low. (Vmax<3.3V)
122	1	Out	HPINT*	**Hot Plug Interrupt Output** This pin provides an open drain output, which pulls low when a termination change has been detected on the HPD input.
36	1	In	VSWING	**LVDS Voltage Swing Control** This pin sets the swing level of the LVDS outputs. A 2.4K Ohm resistor should be connected between this pin and LGND (pin 35) using short and wide traces.
58	1	In	RESET*	**Reset * Input** (Internal Pull-up) When this pin is low, the device is held in the power on reset condition. When this pin is high, reset is controlled through the serial port.
2	1	Analog	LPLLCAP	**LVDS PLL Capacitor** This pins allows coupling of any signal to the on-chip loop filter capacitor.
5, 24	2	Out	LL2C, LL1C	**Positive LVDS differential Clock2 & Clock1**
6, 25	2	Out	LL2C*, LL1C*	**Negative LVDS differential Clock2 & Clock1**
8, 11, 14, 17	4	Out	LDC[7:4]	**Positive LVDS differential data[7:4]**
9, 12, 15, 18	4	Out	LDC[7:4]*	**Negative LVDS differential data[7:4]**
21, 27, 30, 33	4	Out	LDC[3:0]	**Positive LVDS differential data[3:0]**
22, 28, 31, 34	4	Out	LDC[3:0]*	**Negative LVDS differential data [3:0]**
38	1	Analog	ISET	**Current Set Resistor Input** This pin sets the DAC current. A 140 ohm resistor should be connected between this pin and DAC_GND (pin 67) using short and wide traces.
40, 42, 44, 46	4	Out	DACB[3:0]	**DAC Output B** Video Digital-to-Analog outputs. Refer to Sec. 3.3.3 for information regarding supports for Composite Video, S-Video, SCART and RGB Bypass outputs. Each output is capable of driving two 75 ohm (doubly terminated) loads.
41, 43, 45, 47	4	Out	DACA[3:0]	**DAC Output A** Video Digital-to-Analog outputs. Refer to Sec. 3.3.3 for information regarding supports for Composite Video, S-Video, SCART, YPrPb and RGB Bypass outputs. Each output is capable of driving two 75 ohm (doubly terminated) loads.
120	1	Out	VOUT	**V-Sync Output** This pin is the output of a voltage translating digital buffer and is driven from V5V.
110	1	In	VIN	**V-Sync Input** This pin is the input of a voltage translating digital buffer. Input threshold can be programmed by serial port to equal to VREF2/2 or to DVDD/2
119	1	Out	HOUT	**H-Sync Output** This pin is the output of a voltage translating digital buffer and is driven from V5V.
109	1	In	HIN	**H-Sync Input** This pin is the input of a voltage translating digital buffer. Input threshold can be programmed by serial port to equal to VREF2/2 or to DVDD/2
49	1	Out	C/HSYNC	**Composite / Horizontal Sync** Provides composite sync in TV modes and horizontal sync in bypass RGB mode. This pin is driven by the DVDD supply.
50	1	Out	BCO/VSYNC	**Buffered Clock Outputs / Vertical Sync** This output pin provides buffered crystal oscillator clock output or VSYNC output in bypass RGB mode. This pin is driven by the DVDD supply.

Table 1: Pin Description (Continue)

Pin #	# of Pins	Type	Symbol	Description
52	1	In	XI / FIN	**Crystal Input / External Reference Input** A parallel resonant 14.31818MHz crystal (± 20 ppm) should be attached between this pin and XO. However, an external CMOS compatible clock can drive the XI/FIN input.
53	1	Out	XO	**Crystal Output** A parallel resonance 14.31818MHz crystal (± 20 ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
59	1	Out	P-Out	**Pixel Clock Output** This pin provides a pixel clock signal to the VGA controller which can be used as a reference frequency. The output is selectable between 1X or 2X of the pixel clock frequency. The output driver is driven from the VDDV supply. This output has a programmable tri-state. The capacitive loading on this pin should be kept to a minimum.
61	1	In	VREF1	**Reference Voltage Input 2** The VREF pin inputs a reference voltage of VDDV / 2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, sync and clock inputs.
68-73, 77-82	12	In	D1[11:0]	**Data2[11] through Data2[0] Inputs** These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to VDDV. VREF is the threshold level.
76, 74	2	In	XCLK1, XCLK1*	**External Clock Inputs** These inputs form a differential clock signal input to the device for use with the H2, V2 and D2[11:0] data. If differential clocks are not available, the XCLK2* input should be connected to VREF. The clock polarity can be selected by the MCP control bit.
85-90, 94-99	12	In	D2[11:0]	**Data1[11] through Data1[0] Inputs** These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to DVDDV. VREF1 is the threshold level.
93, 91	2	In	XCLK2, XCLK2*	**External Clock Inputs** These inputs form a differential clock signal input to the device for use with the H1, V1 and D1[11:0] data. If differential clocks are not available, the XCLK1* input should be connected to VREF. The clock polarity can be selected by the MCP control bit.
118	1	Power	V5V	**5V supply for H/VOUT** (5V)
64, 83, 84, 103	4	Power	DVDD	**Digital Supply Voltage** (3.3V)
67, 75, 92, 100	4	Power	DGND	**Digital Ground**
60	1	Power	VDDV	**I/O Supply Voltage** (1.1V to 3.3V)
55	2	Power	TVPLL_VDD	**TV PLL Supply Voltage** (3.3V)
54	1	Power	TVPLL_VCC	**TV PLL Supply Voltage** (3.3V)
51	1	Power	TVPLL_GND	**TV PLL Ground**
37	1	Power	DAC_VDD	**DAC Supply Voltage** (3.3V)
39, 48	1	Power	DAC_GND	**DAC Ground**
7, 13, 19, 20, 26, 32	6	Power	LVDD	**LVDS Supply Voltage** (3.3V)
4, 10, 16, 23, 29, 35	6	Power	LGND	**LVDS Ground**
1	1	Power	LPLL_VDD	**LVDS PLL Supply Voltage** (3.3V)
3	1	Power	LPLL_GND	**LVDS PLL Ground**

3.0 Overview

The CH7017 is a VGA to TV encoder with dual LVDS output for the graphics subsystem. Both TV-Out and LVDS-Out can operate simultaneously if the two 12-bit input ports are driven from different timing generators. TV timing requirements are usually different from that of the TFT-LCD panels. If the graphic controller can generate only one set of timing, simultaneous display on both the TV and the flat panel may not be available for all graphic modes. Descriptions of each of the operating modes with block diagrams of the data flow within the device are shown below.

The CH7017 also supports 24-bit input mode by ganging D1 and D2 together as a single 24-bit data port. Either sets of timing timing signals (Hx, Vx , Dex and FLD/STLx) can be enabled. Video data are sent to either the TV encoder (including RGB bypass) or to the LVDS data path, but not both. Maximum data rate supported through the dual LVDS links is 330M Pixels /sec. The maximum pixel rate support by the RGB bypass mode is 165 Mpixels/sec

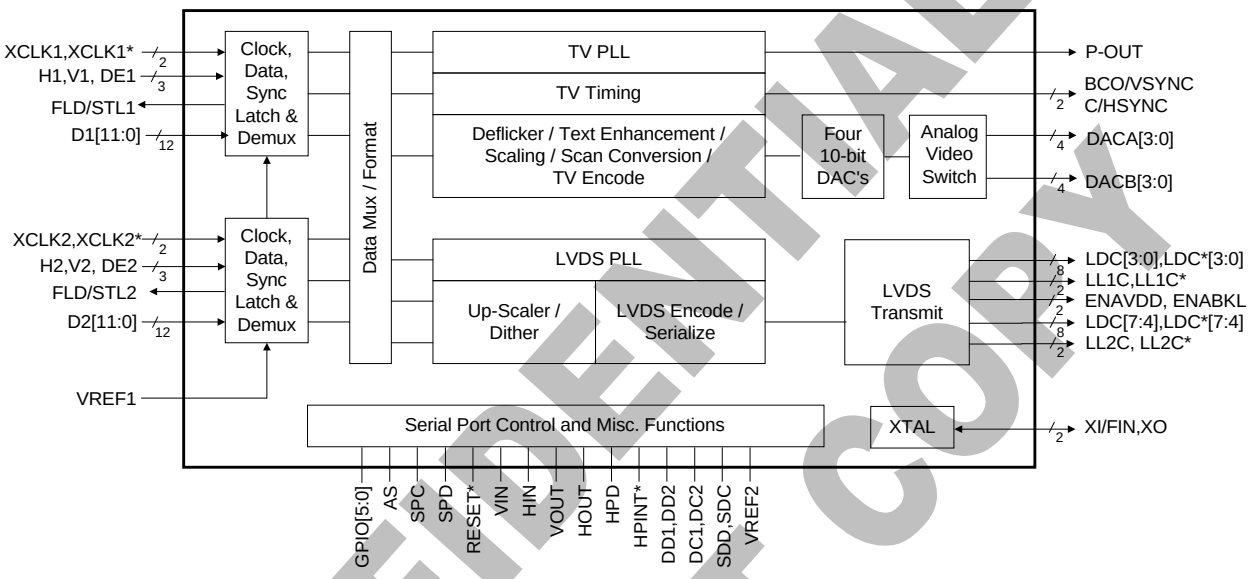

Figure 3: Functional Block Diagram

3.1 Input Interface Timing

Four distinct methods of transferring data to the CH7017 are described below. In each of the four modes, DEx is used to signal active LVDS data for the panel and register SAV value denotes the start of active TV video.

A. 12-bit Multiplexed Data – Dual-edge Transfer

- Multiplexed data - two 12-bit words per pixel from either D1[11:0] or D2[11:0]
- Clock frequency equals 1X pixel rate with 12-bit data transfer at both rising and falling clock edges.
- Maximum pixel rate is 165M pixels per second with a 165 MHz pixel clock.
- Simultaneous TV and panel display.

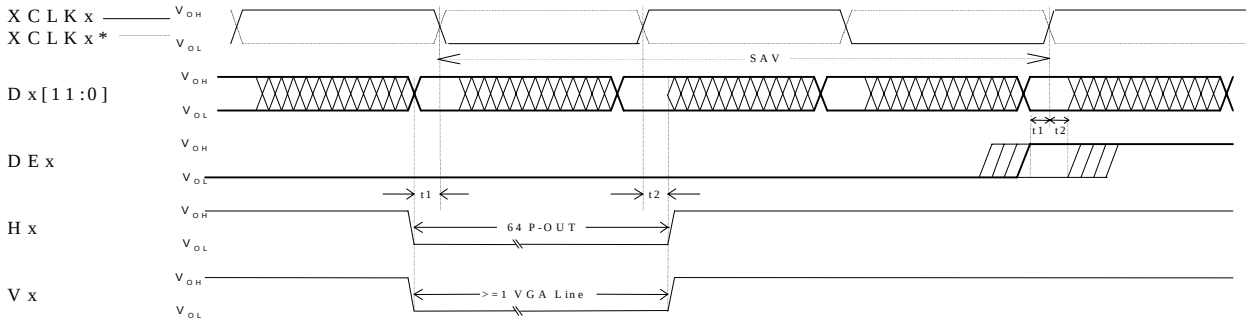

Figure 4: Interface Timing for Multiplexed Data – Dual-edge Transfer

B. 12-bit Multiplexed Data – Single-edge Transfer

- Multiplexed data - two 12-bit words per pixel from either D1[11:0] or D2[11:0]
- Clock frequency equals 2X pixel rate with 12-bit data transfer at either rising or falling edge of clock (programmble via serial port).
- Maximum pixel rate is 165M pixels per second with a 330 MHz pixel clock.
- Simultaneous TV and panel display.

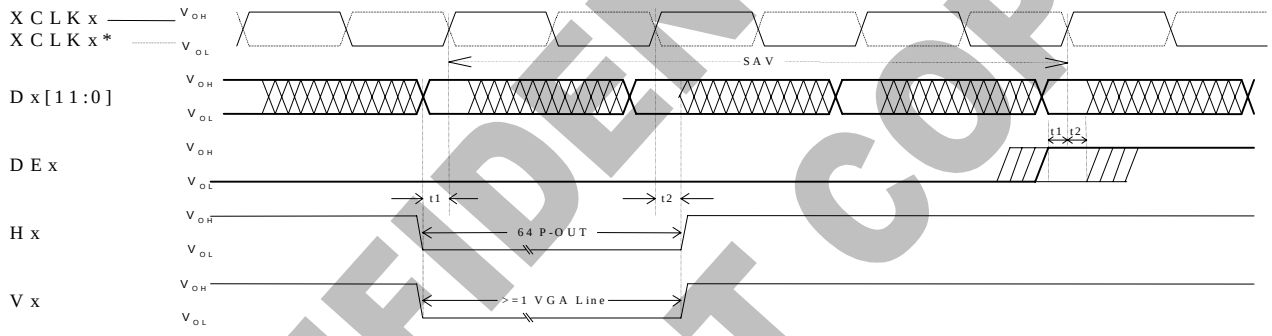

Figure 5: Interface Timing for Multiplexed Data – Single-edge Transfer

C. 24-bit Ganged Data – Dual-edge Transfer

- Multiplexed data - two 24-bit words per pixel from both D1[11:0] and D2[11:0]
- Clock frequency equals 1/2X pixel rate with 24-bit data transfer at both rising and falling clock edges.
- Maximum pixel rate is 330M pixels per second with a 165 MHz pixel clock.
- No Simultaneous TV and panel display.

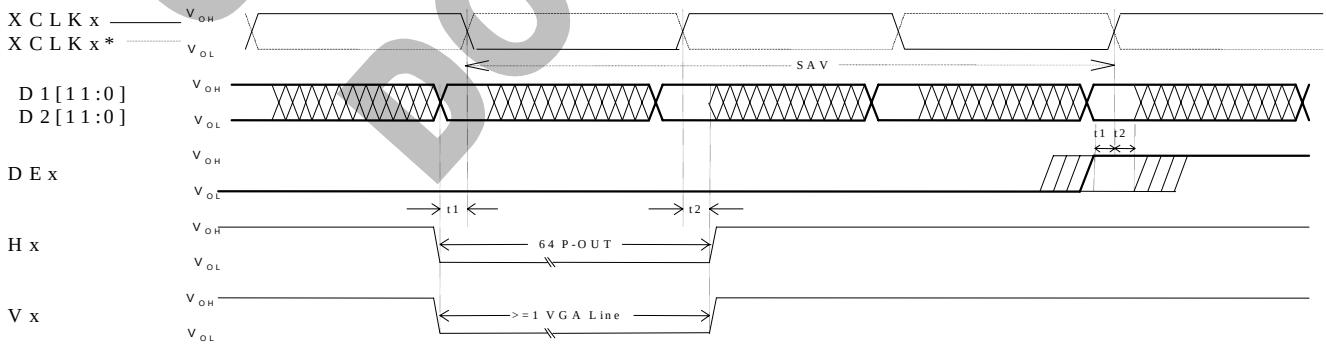

Figure 6: Interface Timing for 24-bit Multiplexed Data – Dual-edge Transfer

D. 24-bit Ganged Data – Single-edge Transfer

- Non-multiplexed data - one 24-bit word per pixel from both D1[11:0] and D2[11:0].
- Clock frequency equals 1X pixel rate with 24-bit data transfer at either rising or falling edge of clock (programmable via serial port).
- Maximum pixel rate is 330M pixels per second with a 330 MHz pixel clock.
- No simultaneous TV and panel display.

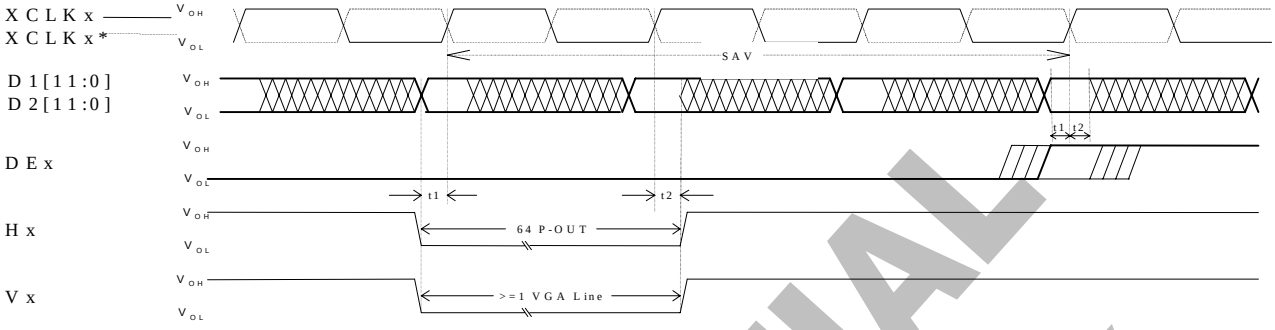

Figure 7: Interface Timing for Non-multiplexed Data – Single-edge Transfer

Table 2: Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	Output high level of interface signals	DVDDV - 0.2	DVDDV	DVDDV + 0.2	V
V_{OL}	Output Low level of interface signals	-0.2	0	0.2	V
t1+t2	Total setup & hold time		.5		nS
t1, t2	Setup time and hold time are programmable through serial port - XCMD [7:0] by delay or advance clock relative to data.	TBD	programmable	TBD	nS
VDDV	Digital I/O Supply Voltage	1.1 – 5%		3.3 + 5%	V

3.2 Input Data Formats

3.2.1 12-Bit Multiplexed Data Formats

Multiplexed pixel data inputs to the CH7017 through D1[11:0] or D2[11:0] using data transfer method A or B described in 3.1. Received data is formatted and sent through an internal data bus P1[23:0] to TV encoder or directly to the TV DAC's, or through bus P2[23:0] to the LVDS data path. The multiplexed input data formats are (IDF[2:0]=0,1,2,3 and 4):

IDF	Description
0	RGB 8-8-8 (2x12-bit)
1	RGB 8-8-8 (2x12-bit) or RGB 5-6-5 (2x8-bit)
2	RGB 5-6-5 (2x8bit)
3	RGB 5-5-5 (2x8-bit)
4	YCrCb 8-8 (2x8-bit)

For multiplexed input data formats, data can be latched from the graphics controller by either rising only or falling only clock edges, or by both rising and falling clock edges. The MCP bit selects the rising or the falling clock edge, where rising refers to rising edge on the XCLK signal and falling edge on the XCLK* signal. The multiplexed input data formats are shown in the Figures 8 and 9 below. The input data bus Dx[11:0], where x can be either 1 or 2, transports a 12-bit or 8-bit multiplexed data stream containing either RGB or YCrCb formatted data. The input data rate is 2X the pixel rate and each pair of Pn values (eg; P0a and P0b) contains a complete pixel encoded as shown in the tables 3 to 6 below and can be placed onto one or both of the internal pixel buses Py[23:0], where y equals 1 or 2. It is assumed that the first clock cycle following the leading edge of the incoming horizontal sync signal contains the first word (Pxa) of a pixel, if an active pixel was present immediately following the horizontal sync. When the input is a YCrCb data stream the color-difference data will be transmitted at half the data rate of the luminance data with the sequence being set as Cb, Y, Cr, Y, where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples and the following Y1 byte refers to the next luminance sample, per CCIR-656 standards (the clock frequency is dependent upon the current mode, and is not 27MHz as specified in CCIR-656). All non-active pixels should be 0 in RGB formats, and 16 for Y and 128 for CrCb in YCrCb formats.

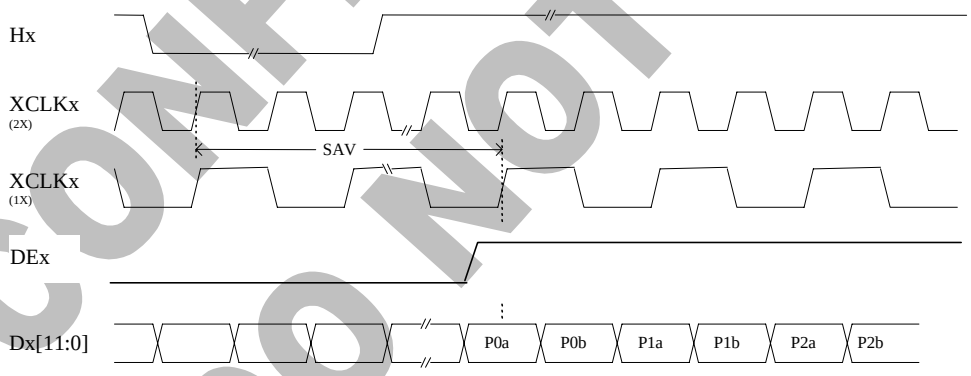

Figure 8: 12-bit Multiplexed Input Data Formats (IDF = 0,1,2,3,4,5)

Table 3: Multiplexed Input Data Formats (IDF = 0, 1)

IDF = Format =		0 RGB 8-8-8 (2x12-bit) For TV/Bypass RGB or/and LVDS				1 RGB 8-8-8 (2x12-bit) or RGB 5-6-5 (2x8-bit) For TV/Bypass RGB or/and LVDS			
Pixel #		P0a	P0b	P1a	P1b	P0a	P0b	P1a	P1b
Bus Data	Dx[11]	G0[3]	R0[7]	G1[3]	R1[7]	G0[4]	R0[7]	G1[4]	R1[7]
	Dx[10]	G0[2]	R0[6]	G1[2]	R1[6]	G0[3]	R0[6]	G1[3]	R1[6]
	Dx[9]	G0[1]	R0[5]	G1[1]	R1[5]	G0[2]	R0[5]	G1[2]	R1[5]
	Dx[8]	G0[0]	R0[4]	G1[0]	R1[4]	B0[7]	R0[4]	B1[7]	R1[4]
	Dx[7]	B0[7]	R0[3]	B1[7]	R1[3]	B0[6]	R0[3]	B1[6]	R1[3]
	Dx[6]	B0[6]	R0[2]	B1[6]	R1[2]	B0[5]	G0[7]	B1[5]	G1[7]
	Dx[5]	B0[5]	R0[1]	B1[5]	R1[1]	B0[4]	G0[6]	B1[4]	G1[6]
	Dx[4]	B0[4]	R0[0]	B1[4]	R1[0]	B0[3]	G0[5]	B1[3]	G1[5]
	Dx[3]	B0[3]	G0[7]	B1[3]	G1[7]	G0[0]	R0[2]	G1[0]	R1[2]
	Dx[2]	B0[2]	G0[6]	B1[2]	G1[6]	B0[2]	R0[1]	B1[2]	R1[1]
	Dx[1]	B0[1]	G0[5]	B1[1]	G1[5]	B0[1]	R0[0]	B1[1]	R1[0]
	Dx[0]	B0[0]	G0[4]	B1[0]	G1[4]	B0[0]	G0[1]	B1[0]	G1[1]

Table 4: Multiplexed Input Data Formats (IDF = 2, 3)

IDF = Format =		2 RGB 5-6-5 (2x8bit) for TV/Bypass RGB or/and LVDS				3 RGB 5-5-5 (2x8-bit) for TV/Bypass RGB or/and LVDS			
Pixel #		P0a	P0b	P1a	P1b	P0a	P0b	P1a	P1b
Bus Data	Dx[11]	G0[4]	R0[7]	G1[4]	R1[7]	G0[5]	X	G1[5]	X
	Dx[10]	G0[3]	R0[6]	G1[3]	R1[6]	G0[4]	R0[7]	G1[4]	R1[7]
	Dx[9]	G0[2]	R0[5]	G1[2]	R1[5]	G0[3]	R0[6]	G1[3]	R1[6]
	Dx[8]	B0[7]	R0[4]	B1[7]	R1[4]	B0[7]	R0[5]	B1[7]	R1[5]
	Dx[7]	B0[6]	R0[3]	B1[6]	R1[3]	B0[6]	R0[4]	B1[6]	R1[4]
	Dx[6]	B0[5]	G0[7]	B1[5]	G1[7]	B0[5]	R0[3]	B1[5]	R1[3]
	Dx[5]	B0[4]	G0[6]	B1[4]	G1[6]	B0[4]	G0[7]	B1[4]	G1[7]
	Dx[4]	B0[3]	G0[5]	B1[3]	G1[5]	B0[3]	G0[6]	B1[3]	G1[6]

Table 5: Multiplexed Input Data Formats (IDF = 4)

IDF = Format =		4 YCrCb 4:2:2 (2x8-bit) for TV							
Pixel #		P0a	P0b	P1a	P1b	P2a	P2b	P3a	P3b
Bus Data	Dx[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	Dx[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	Dx[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	Dx[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	Dx[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	Dx[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	Dx[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	Dx[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

When IDF = 4 (YCrCb mode), the data inputs can also be used to transmit sync information to the device. In this mode, the embedded sync will follow the VIP2 convention, and the first byte of the 'video timing reference code' will be assumed to occur when a Cb sample would occur, if the video stream was continuous. This is shown below:

Table 6: Multiplexed Input Data Formats (IDF = 4) with Embedded Sync

IDF = Format =		4 YCrCb 4:2:2 (2x8-bit) for TV							
Pixel #		P0a	P0b	P1a	P1b	P2a	P2b	P3a	P3b
Bus Data	Dx[7]	FF	00	00	S[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	Dx[6]	FF	00	00	S[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	Dx[5]	FF	00	00	S[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	Dx[4]	FF	00	00	S[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	Dx[3]	FF	00	00	S[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	Dx[2]	FF	00	00	S[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	Dx[1]	FF	00	00	S[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	Dx[0]	FF	00	00	S[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

In this mode, the S[7..0] byte contains the following data:
S[6] = F = 1 during field 2, 0 during field 1
S[5] = V = 1 during field blanking, 0 elsewhere
S[4] = H = 1 during EAV (synchronization reference at the end of active video)
0 during SAV (synchronization reference at the start of active video)
S[7] and S[3:0] are ignored

3.2.2 24-Bit Data Formats

The two 12-bit input data ports, D1[11:0] and D2[11:0], can be grouped together to form a single 24-bit interface to the graphic controller. Either set of timing signals (Hx, Vx, DEx, XCLKx and XCLK*x) can be chosen as the active signal by programming register X. The CH7017 supports 5 different 24-bit data formats. Each of which can be used with a 1X pixel rate clock latching data with one of the clock edges or with a 1/2X pixel rate clock latching data with both the rising and the falling edge. The 24-bit input data formats are (IDF[2:0]=5,6, 7 and 8):

IDF	Description
5	RGB 8-8-8 (1x24-bit) for TV/Bypass RGB
6	YCrCb 8-8-8 (1x24-bit) for TV
7	YCrCb 8-8 (1x16-bit with CrCb multiplexed and decimated by 2) for TV
8	RGB 8-8-8 (1x24-bit) Normal Ganged for LVDS
9	RGB 8-8-8 (2x24-bit) Odd / Even Ganged for LVDS

The pixel data bus represents a 24-bit or 16-bit data stream containing either RGB or YCrCb formatted data. When the input is a 16-bit YCrCb data stream the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb0, Y0 transmitted during one clock cycle, followed by Cr0, Y1 the following clock cycle, where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples and the Y1 data refers to the next luminance sample, per CCIR-601 sampling. Non-active data must be 0 in RGB format, and 16 for Y, 128 for Cr and Cb in YCrCb formats.

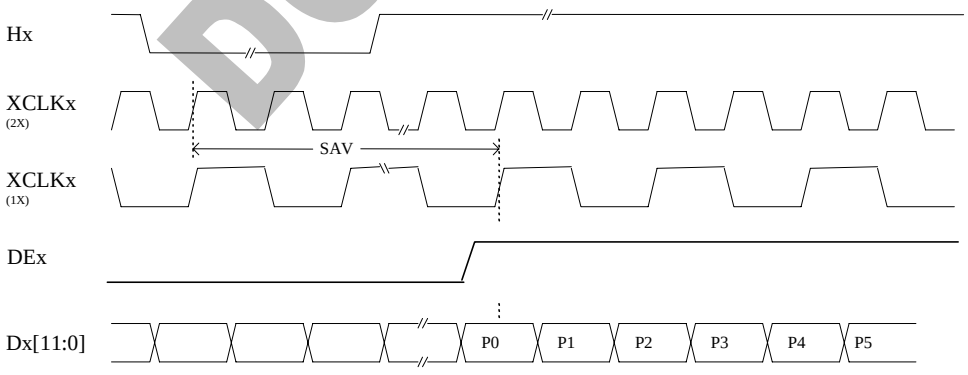

Figure 9: Multiplexed Input Data Formats (IDF = 5,6,7,8)

Ta**ble 7: Non-Multiplexed Data Formats**

IDF = Format =		**5 24-bit RGB for for TV/Bypass RGB**		**6 24-bit YCrCb for TV**		**7 16-bit YCrCb for TV**			
Pixel #		**P0**	**P1**	**P0**	**P1**	**P0**	**P1**	**P2**	**P3**
Bus Data	D1[11]	R0[7]	R1[7]	Y0[7]	Y1[7]	Y0[7]	Y1[7]	Y2[7]	Y3[7]
	D1[10]	R0[6]	R1[6]	Y0[6]	Y1[6]	Y0[6]	Y1[6]	Y2[6]	Y3[6]
	D1[9]	R0[5]	R1[5]	Y0[5]	Y1[5]	Y0[5]	Y1[5]	Y2[5]	Y3[5]
	D1[8]	R0[4]	R1[4]	Y0[4]	Y1[4]	Y0[4]	Y1[4]	Y2[4]	Y3[4]
	D1[7]	R0[3]	R1[3]	Y0[3]	Y1[3]	Y0[3]	Y1[3]	Y2[3]	Y3[3]
DVOB	D1[6]	R0[2]	R1[2]	Y0[2]	Y1[2]	Y0[2]	Y1[2]	Y2[2]	Y3[2]
	D1[5]	R0[1]	R1[1]	Y0[1]	Y1[1]	Y0[1]	Y1[1]	Y2[1]	Y3[1]
	D1[4]	R0[0]	R1[0]	Y0[0]	Y1[0]	Y0[0]	Y1[0]	Y2[0]	Y3[0]
	D1[3]	G0[7]	G1[7]	Cr0[7]	Cr1[7]	Cb0[7]	Cr0[7]	Cb2[7]	Cr2[7]
	D1[2]	G0[6]	G1[6]	Cr0[6]	Cr1[6]	Cb0[6]	Cr0[6]	Cb2[6]	Cr2[6]
	D1[1]	G0[5]	G1[5]	Cr0 [5]	Cr1 [5]	Cb0 [5]	Cr0 [5]	Cb2 [5]	Cr2 [5]
	D1[0]	G0[4]	G1[4]	Cr0 [4]	Cr1 [4]	Cb0 [4]	Cr0 [4]	Cb2 [4]	Cr2 [4]
	D2[11]	G0[3]	G1[3]	Cr0 [3]	Cr1 [3]	Cb0 [3]	Cr0 [3]	Cb2 [3]	Cr2 [3]
	D2[10]	G0[2]	G1[2]	Cr0 [2]	Cr1 [2]	Cb0 [2]	Cr0 [2]	Cb2 [2]	Cr2 [2]
	D2[9]	G0[1]	G1[1]	Cr0 [1]	Cr1 [1]	Cb0 [1]	Cr0 [1]	Cb2 [1]	Cr2 [1]
	D2[8]	G0[0]	G1[0]	Cr0 [0]	Cr1 [0]	Cb0 [0]	Cr0 [0]	Cb2 [0]	Cr2 [0]
	D2[7]	B0[7]	B1[7]	Cb0[7]	Cb1[7]				
DVOC	D2[6]	B0[6]	B1[6]	Cb0[6]	Cb1[6]				
	D2[5]	B0[5]	B1[5]	Cb0 [5]	Cb1[5]				
	D2[4]	B0[4]	B1[4]	Cb0 [4]	Cb1[4]				
	D2[3]	B0[3]	B1[3]	Cb0 [3]	Cb1[3]				
	D2[2]	B0[2]	B1[2]	Cb0 [2]	Cb1[2]				
	D2[1]	B0[1]	B1[1]	Cb0 [1]	Cb1[1]				
	D2[0]	B0[0]	B1[0]	Cb0 [0]	Cb1[0]				

When IDF = 6 or 7 (YCrCb modes), the data inputs can be used to transmit sync information to the device. For 16-bit mode, the embedded sync follows the VIP2 convention, and the first byte of the video timing reference code is assumed to occur when a Cb sample occurs, if the video stream is continuous. This is shown in Table 8 below.

Table 8: Non-Multiplexed YCrCb modes with Embedded Sync

IDF = Format =		**6 24-bit YcrCb for TV**				**7 16-bit YcrCb for TV**			
Pixel #		**P0**	**P1**	**P2**	**P3**	**P0**	**P1**	**P2**	**P3**
Bus Data	D1[11]	0	S[7]	Y0[7]	Y1[7]	0	S[7]	Y0[7]	Y1[7]
	D1[10]	0	S[6]	Y0[6]	Y1[6]	0	S[6]	Y0[6]	Y1[6]
	D1[9]	0	S[5]	Y0[5]	Y1[5]	0	S[5]	Y0[5]	Y1[5]
	D1[8]	0	S[4]	Y0[4]	Y1[4]	0	S[4]	Y0[4]	Y1[4]
	D1[7]	0	S[3]	Y0[3]	Y1[3]	0	S[3]	Y0[3]	Y1[3]
	D1[6]	0	S[2]	Y0[2]	Y1[2]	0	S[2]	Y0[2]	Y1[2]
	D1[5]	0	S[1]	Y0[1]	Y1[1]	0	S[1]	Y0[1]	Y1[1]
	D1[4]	0	S[0]	Y0[0]	Y1[0]	0	S[0]	Y0[0]	Y1[0]
	D1[3]	FF	X	Cb0[7]	Cb1[7]	FF	0	Cb0[7]	Cr0[7]
	D1[2]	FF	X	Cb0[6]	Cb1[6]	FF	0	Cb0[6]	Cr0[6]
	D1[1]	FF	X	Cb0 [5]	Cb1[5]	FF	0	Cb0 [5]	Cr0 [5]
	D1[0]	FF	X	Cb0 [4]	Cb1[4]	FF	0	Cb0 [4]	Cr0 [4]
	D2[11]	FF	X	Cb0 [3]	Cb1[3]	FF	0	Cb0 [3]	Cr0 [3]
	D2[10]	FF	X	Cb0 [2]	Cb1[2]	FF	0	Cb0 [2]	Cr0 [2]
	D2[9]	FF	X	Cb0 [1]	Cb1[1]	FF	0	Cb0 [1]	Cr0 [1]
	D2[8]	FF	X	Cb0 [0]	Cb1[0]	FF	0	Cb0 [0]	Cr0 [0]
	D2[7]	0	X	Cr0[7]	Cr1[7]				
	D2[6]	0	X	Cr0[6]	Cr1[6]				
	D2[5]	0	X	Cr0 [5]	Cr1 [5]				
	D2[4]	0	X	Cr0 [4]	Cr1 [4]				
	D2[3]	0	X	Cr0 [3]	Cr1 [3]				
	D2[2]	0	X	Cr0 [2]	Cr1 [2]				
	D2[1]	0	X	Cr0 [1]	Cr1 [1]				
	D2[0]	0	X	Cr0 [0]	Cr1 [0]				

In this mode, the S[7..0] byte contains the following data:
S[6] = F = 1 during field 2, 0 during field 1
S[5] = V = 1 during field blanking, 0 elsewhere
S[4] = H = 1 during EAV (synchronization reference at the end of active video)
0 during SAV (synchronization reference at the start of active video)
S[7] and S[3:0] are ignored

Under mode 8 and 9, the CH7017 takes 24-bit data from both D1 and D2 and outputs to the dual LVDS links. A maximum through put of 330M pixels per second can be achieved. The timing signals of both input ports are identical. H1, V1 and XCLK1 equal H2, V2 and XCLK2, respectively. Up-scaling and dithering functions are not available in these modes.

IDF = Format =		**8 24-bit RGB Normal Ganged for LVDS**		**9 24-bit RGB Odd/Even Ganged for LVDS**	
Pixel #		**P0**	**P1**	**P0**	**P1**
Bus Data	D1[11]	R0[7]	R1[7]	G0[3]	R0[7]
	D1[10]	R0[6]	R1[6]	G0[2]	R0[6]
	D1[9]	R0[5]	R1[5]	G0[1]	R0[5]
	D1[8]	R0[4]	R1[4]	G0[0]	R0[4]
	D1[7]	R0[3]	R1[3]	B0[7]	R0[3]
DVOB	D1[6]	R0[2]	R1[2]	B0[6]	R0[2]
	D1[5]	R0[1]	R1[1]	B0[5]	R0[1]
	D1[4]	R0[0]	R1[0]	B0[4]	R0[0]
	D1[3]	G0[7]	G1[7]	B0[3]	G0[7]
	D1[2]	G0[6]	G1[6]	B0[2]	G0[6]
	D1[1]	G0[5]	G1[5]	B0[1]	G0[5]
	D1[0]	G0[4]	G1[4]	B0[0]	G0[4]
	D2[11]	G0[3]	G1[3]	G1[3]	R1[7]
	D2[10]	G0[2]	G1[2]	G1[2]	R1[6]
	D2[9]	G0[1]	G1[1]	G1[1]	R1[5]
	D2[8]	G0[0]	G1[0]	G1[0]	R1[4]
	D2[7]	B0[7]	B1[7]	B1[7]	R1[3]
DVOC	D2[6]	B0[6]	B1[6]	B1[6]	R1[2]
	D2[5]	B0[5]	B1[5]	B1[5]	R1[1]
	D2[4]	B0[4]	B1[4]	B1[4]	R1[0]
	D2[3]	B0[3]	B1[3]	B1[3]	G1[7]
	D2[2]	B0[2]	B1[2]	B1[2]	G1[6]
	D2[1]	B0[1]	B1[1]	B1[1]	G1[5]
	D2[0]	B0[0]	B1[0]	B1[0]	G1[4]

3.3 TV-Out

Multiplexed input data, sync and clock signals from the graphics controller inputs to the CH7017 through one of the two 12-bit variable voltage input ports, D1[11:0] or D2[11:0], and directed to the TV data path. Non-multiplexed 24-bit input data also inputs through both of the two input ports. Detailed descriptions of the six input data formats are given in Section 3.2. Clock signal (P-Out) outputs as a frequency reference to the graphics controller to ensure accurate frequency generation. Horizontal and vertical sync signals are normally sent to the CH7017 from the graphics controller, but can be optionally generated by the CH7017 and output to the graphics controller. Using the serial port, the CH7017 can be programmed as the clock master, clock slave, sync master or sync slave. Data will be 2X multiplexed (2x12 bits) or non-multiplexed (1x24 bits), and the XCLK clock signal can be 1X or 2X times the pixel rate. The input data will be encoded into the selected video standard, and output from the video DAC's. The modes supported for TV-Out are shown in the table 9 below.

Table 9: TV Output Modes

Graphics Resolution	Active Aspect Ratio	Pixel Aspect Ratio	TV Output Standard	Scaling Ratios
512x384	4:3	1:1	PAL	5/4, 1/1
512x384	4:3	1:1	NTSC	5/4, 1/1
720x400	4:3	1.35:1.00	PAL	5/4, 1/1
720x400	4:3	1.35:1.00	NTSC	5/4, 1/1
640x400	8:5	1:1	PAL	5/4, 1/1
640x400	8:5	1:1	NTSC	5/4, 1/1, 7/8
640x480	4:3	1:1	PAL	5/4, 1/1, 5/6
640x480	4:3	1:1	NTSC	1/1, 7/8, 5/6
720x480[1]	4:3	9:8	NTSC	1/1
720x480[2]	4:3	9:8	NTSC	1/1, 7/8, 5/6
720x576[1]	4:3	15:12	PAL	1/1
720x576[2]	4:3	15:12	PAL	1/1, 5/6, 5/7
800x600	4:3	1:1	PAL	1/1, 5/6, 5/7
800x600	4:3	1:1	NTSC	3/4, 7/10, 5/8
1024x768	4:3	1:1	PAL	5/7, 5/8, 5/9
1024x768	4:3	1:1	NTSC	5/8, 5/9, 1/2

[1] These DVD modes operate with interlaced input. Scan conversion and flicker filter are bypassed.
[2] These DVD modes operate with non-interlaced input. Scan conversion and flicker filter are not bypassed.

3.3.1 Adaptive Flicker Filter

Same as CH7009

3.3.2 Scaling and Scan Conversion

Same as CH7009

3.3.3 TV Encoder / Bypass RGB / Component Video Outputs

The four TV encoder DAC outputs are switched to two sets of output pins DACA[3:0] and DACB[3:0] via two video switches. This feature facilitates simple connection to two sets of video connectors.

Table 10: TV Outputs Configurations

	2 RCA + 1 S-Video	**SCART**
DACA0 (pin 41)	CVBS	CVBS
DACA1 (pin 43)	Y	G
DACA2 (pin 45)	C	R
DACA3 (pin 47)	CVBS	B
	VGA – Bypass RGB	**HDTV**
DACB0 (pin 40)		
DACB1 (pin 42)	G	Y
DACB2 (pin 44)	R	Pr
DACB3 (pin 46)	B	Pb

The TV Encoder can be bypassed and input data drives the DACs directly. This mode can go to 165 MP/s. The CH7017 supports YPrPb output for driving 480I TV sets and SCART RGB for European TV.

3.4 LVDS-Out

Multiplexed input data, sync and clock signals from the graphics controllers input to the CH7017 through one of the two 12-bit variable voltage input ports, D1[11:0] or D2[11:0]. Non-multiplexed 24-bit input data input through both of the two input ports. Input data can be sent to the LVDS data path and optionally also to the DAC's in the TV data path. The DAC's can output these data at 165 M pixels/sec to drive a second CRT monitor. The clock inputs can be 1X or 2X times the pixel rate. For correct LVDS operation, the input data format must be selected to be one of the RGB 8-8-8 input formats. That is IDF=0, 1, 5, or 6.

3.4.1 Single LVDS Channel Signal Mapping

Table 12: Signal Mapping for Single LVDS Channel

	18-bit	**24-bit SPWG**	**24-bit OpenLDI**
LDC[0](1)	R0	R0	R2
LDC[0](2)	R1	R1	R3
LDC[0](3)	R2	R2	R4
LDC[0](4)	R3	R3	R5
LDC[0](5)	R4	R4	R6
LDC[0](6)	R5	R5	R7
LDC[0](7)	G0	G0	G2
LDC[1](1)	G1	G1	G3
LDC[1](2)	G2	G2	G4
LDC[1](3)	G3	G3	G5
LDC[1](4)	G4	G4	G6
LDC[1](5)	G5	G5	G7
LDC[1](6)	B0	B0	B2
LDC[1](7)	B1	B1	B3
LDC[2](1)	B2	B2	B4
LDC[2](2)	B3	B3	B5
LDC[2](3)	B4	B4	B6
LDC[2](4)	B5	B5	B7
LDC[2](5)	HSYNC	HSYNC	HSYNC
LDC[2](6)	VSYNC	VSYNC	VSYNC
LDC[2](7)	DE	DE	DE

LDC[3](1)		R6	R0
LDC[3](2)		R7	R1
LDC[3](3)		G6	G0
LDC[3](4)		G7	G1
LDC[3](5)		B6	B0
LDC[3](6)		B7	B1
LDC[3](7)		RES	RES

3.4.2 Dual LVDS Channel Signal Mapping

Table 13: Signal Mapping for Single LVDS Channel

	18-bit	24-bit SPWG	24-bit OpenLDI
LDC[0](1)	Ro0	Ro0	Ro2
LDC[0](2)	Ro1	Ro1	Ro3
LDC[0](3)	Ro2	Ro2	Ro4
LDC[0](4)	Ro3	Ro3	Ro5
LDC[0](5)	Ro4	Ro4	Ro6
LDC[0](6)	Ro5	Ro5	Ro7
LDC[0](7)	Go0	Go0	Go2
LDC[1](1)	Go1	Go1	Go3
LDC[1](2)	Go2	Go2	Go4
LDC[1](3)	Go3	Go3	Go5
LDC[1](4)	Go4	Go4	Go6
LDC[1](5)	Go5	Go5	Go7
LDC[1](6)	Bo0	Bo0	Bo2
LDC[1](7)	Bo1	Bo1	Bo3
LDC[2](1)	Bo2	Bo2	Bo4
LDC[2](2)	Bo3	Bo3	Bo5
LDC[2](3)	Bo4	Bo4	Bo6
LDC[2](4)	Bo5	Bo5	Bo7
LDC[2](5)	HSNC	HSYNC	HSYNC
LDC[2](6)	VSYNC	VSYNC	VSYNC
LDC[2](7)	DE	DE	DE
LDC[3](1)		Ro6	Ro0
LDC[3](2)		Ro7	Ro1
LDC[3](3)		Go6	Go0
LDC[3](4)		Go7	Go1
LDC[3](5)		Bo6	Bo0
LDC[3](6)		Bo7	Bo1
LDC[3](7)		RES	RES
LDC[4](1)	Re0	Re0	Re2
LDC[4](2)	Re1	Re1	Re3
LDC[4](3)	Re2	Re2	Re4
LDC[4](4)	Re3	Re3	Re5
LDC[4](5)	Re4	Re4	Re6
LDC[4](6)	Re5	Re5	Re7
LDC[4](7)	Ge0	Ge0	Ge2
LDC[5](1)	Ge1	Ge1	Ge3
LDC[5](2)	Ge2	Ge2	Ge4
LDC[5](3)	Ge3	Ge3	Ge5
LDC[5](4)	Ge4	Ge4	Ge6
LDC[5](5)	Ge5	Ge5	Ge7
LDC[5](6)	Be0	Be0	Be2
LDC[5](7)	Be1	Be1	Be3
LDC[6](1)	Be2	Be2	Be4

LDC[6](2)	Be3	Be3	Be5
LDC[6](3)	Be4	Be4	Be6
LDC[6](4)	Be5	Be5	CNTLE
LDC[6](5)	HSYNC	HSYNC	CNTLF
LDC[6](6)	VSYNC	VSYNC	VSYNC
LDC[6](7)	DE	DE	RES
LDC[7](1)		Re6	Re0
LDC[7](2)		Re7	Re1
LDC[7](3)		Ge6	Ge0
LDC[7](4)		Ge7	Ge1
LDC[7](5)		Be6	Be0
LDC[7](6)		Be7	Be1
LDC[7](7)		RES	RES

3.4.3 Panel Fitting Up-Scaler

The Up-scaler in CH7017 supports the following panel sizes:

Table 14: Popular Panel Sizes

UXGA	1600x1200
SXGA+	1400x1050
	1360x1024
SXGA	1280x1024
	1280x960
XGA	1024x768
	1024x600
SVGA	800x600

The CH7017 can scale incoming graphics data from lower resolution graphics modes supported by the graphics controller to the native resolution of the supported panels. The up-scaler periodically sends a STALL signal to the graphics controller to halt transmission of one line of active video data. The Up-scaler performs 2D interpolation of the graphics input data and does not change pixel rate between input and output. Maximum pixel rate supported by the Up-scaler is 165 M Pixels / sec. This function must be bypassed if pixel rate exceeds 165Hz, as in the Gang modes (IDF=5 or 6 running at 350MP/s). During system boot up, CH7017 relies on graphics controller to provide pixel data at the panel native data rate on the right line and start position such that the WINDOWS logo can be center on the display panel.

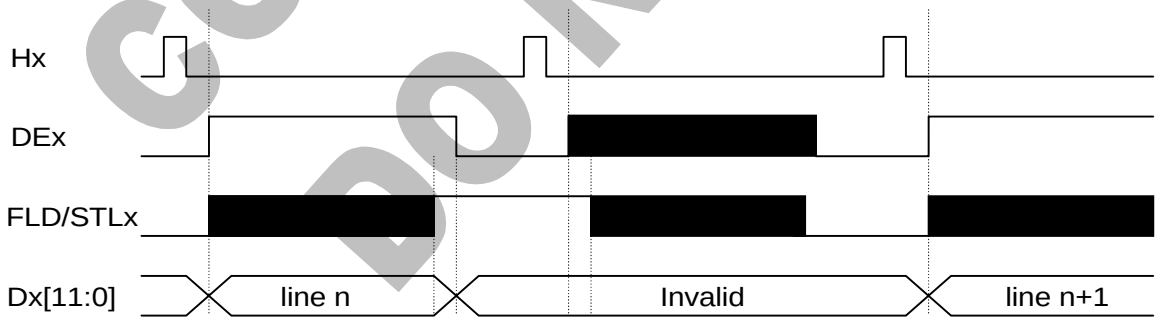

Figure 10: Stall Signal Timing

The up-scaler supports the following scaling algorithms:

- Bilinear interpolation (default)
- Programmable non-linear interpolation

3.4.4. Dithering

The dither engine in the CH7017 converts 24-bit per pixel to 18-bit per pixel RGB data before sending to the LVDS encoder. The 1D or the 2D dither algorithm can be selected via serial port programming. Maximum pixel rate supported is 165 M Pixels / sec. This function must be bypassed when pixel rate exceeds 165MHz.

3.4.5 Power Sequencing

The CH7017 conforms to SPWG's requirements on power sequencing. The timing specification shown in Figure 12 is a superset of the requirements dictated by the SPWG specification. The timing parameters can be programmed to different values via the serial port to suit requirements by different panels.

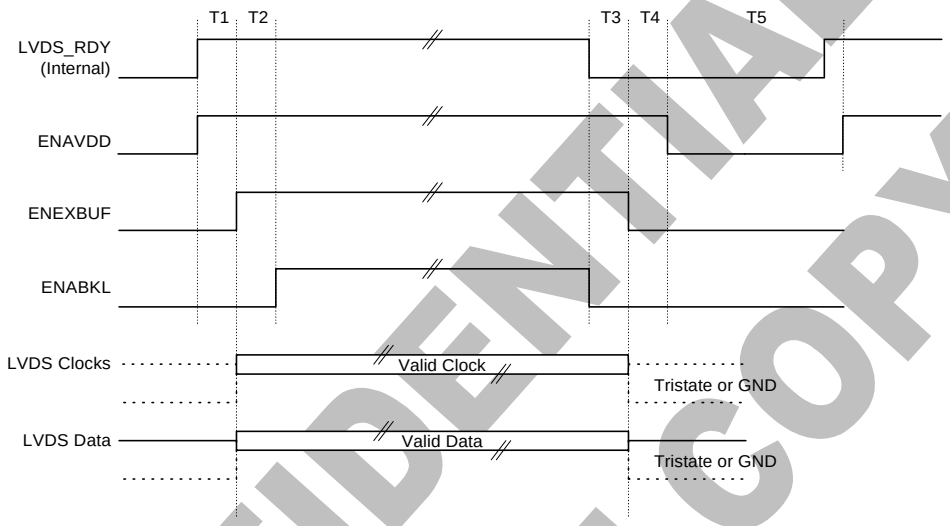

Figure 11 : Power Sequencing

Table 15: Power Sequencing

	Range	Increment
T1	0-512 ms	1 ms
T2	0-256 ms	2ms
T3	0-256 ms	2ms
T4	0-512 ms	1 ms
T5	0-400 ms	100 ms

Power-on sequence begins when the LVDS software registers are set properly via serial port and the LVDS_RDY signal is set by the internal PLL lock detection circuit and the internal Sync detection circuits. Power-off sequence begins when any detection circuits are set (please refer to 3.4.6), or through software programming. Once power-off sequence starts, the internal state machine would complete the sequence and power-on sequence is allowed only after T5 is passed.

When the LVDS clock and data signals become invalid, these outputs are tri-stated or grounded depending on software register LOTG[1:0] setting.

3.4.6 Panel Protection

LCD panel can be damaged if H sync is absent from the LVDS link. This situation can happen when there is a catastrophic failure in the PC or the graphics system. The CH7017 is designed to prevent damages to the panel under such failure. If the system fails, the CH7017 does not expect any software instruction from the graphics controller to power down the panel. Detection circuits are used to monitor the three timing signals – Hsync, Vsync and Xclk. If any

one, combinations of , or all of these signals becomes unstable, the CH7017 will commence Power Down Sequencing according to section 3.4.5. A description of these detection circuits is shown in Figure 13.

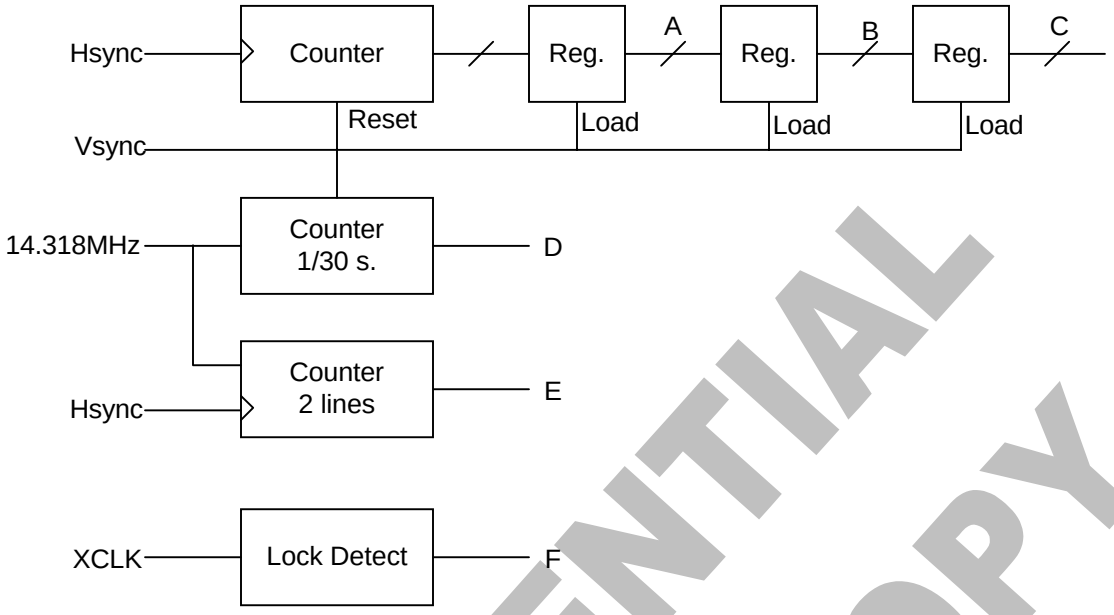

Figure 12 Detection Circuits for Panel Protection

A counter is used to count the number of Hsync per frame. If the end counts A, B, and C are the same, CH7017 will commence Power Up Sequence. If Hsync is not stable resulting in different end counts, i.e. A is not equal to B or C, then CH7017 will commence Power Down Sequence. CH7017 will also go into Power Down Sequence if Vsync is missing for 2 frames (D=1) , Hsync is missing for 2 lines (E=1), or XCLK is not stable (F=1). The stability of XCLK is determined by the number of PLL unlock signal generated within one frame. This number is programmable via serial port. Under software control, outputs of these detection circuits can be forced to 0 or ignored by the power sequencing circuits.

3.4.7 Spread Spectrum Clock

LVDS data path can support a +- 2.5% spread spectrum clock to reduce EMI emission. Details to be released.

3.5 Misc. Functions

3.5.1 Voltage Buffering for H and V Syncs

Two 5-volt non-inverting buffers are included so that the graphics controller can output low-voltage Hsync and Vsync signals to the CH7017, which in-turn outputs a 5V sync signal to the CRT monitor. Input threshold voltage for these buffers is programmable via serial port to be equal to DVDD/2 or to VREF2/2.

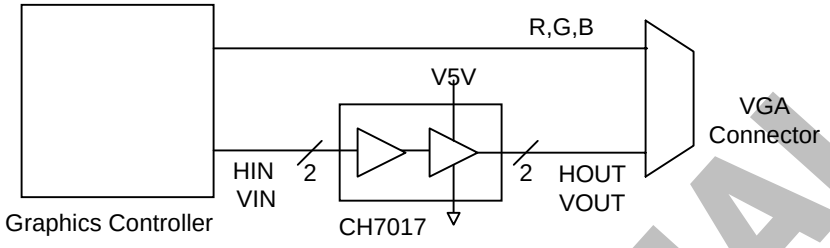

Figure 13 H and V Sync Buffers

3.5.2 Voltage Translation Buffers

DDC's for VGA and flat panels are typically terminated into 5V. CH7017 can translate a low-voltage DDC signal into a 5V DDC signal and vice-versa. Eliminating the use of external MOSFET's for such function.

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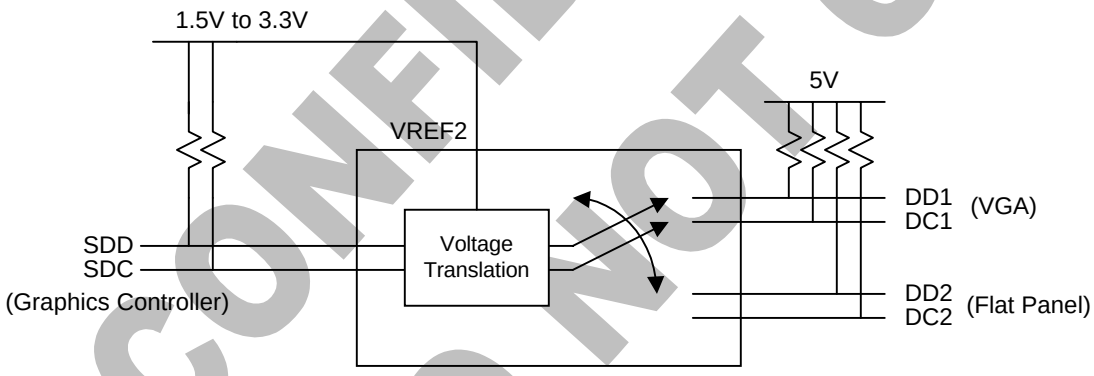

Figure 14 Voltage Translation Buffers

4.0 Package Dimensions

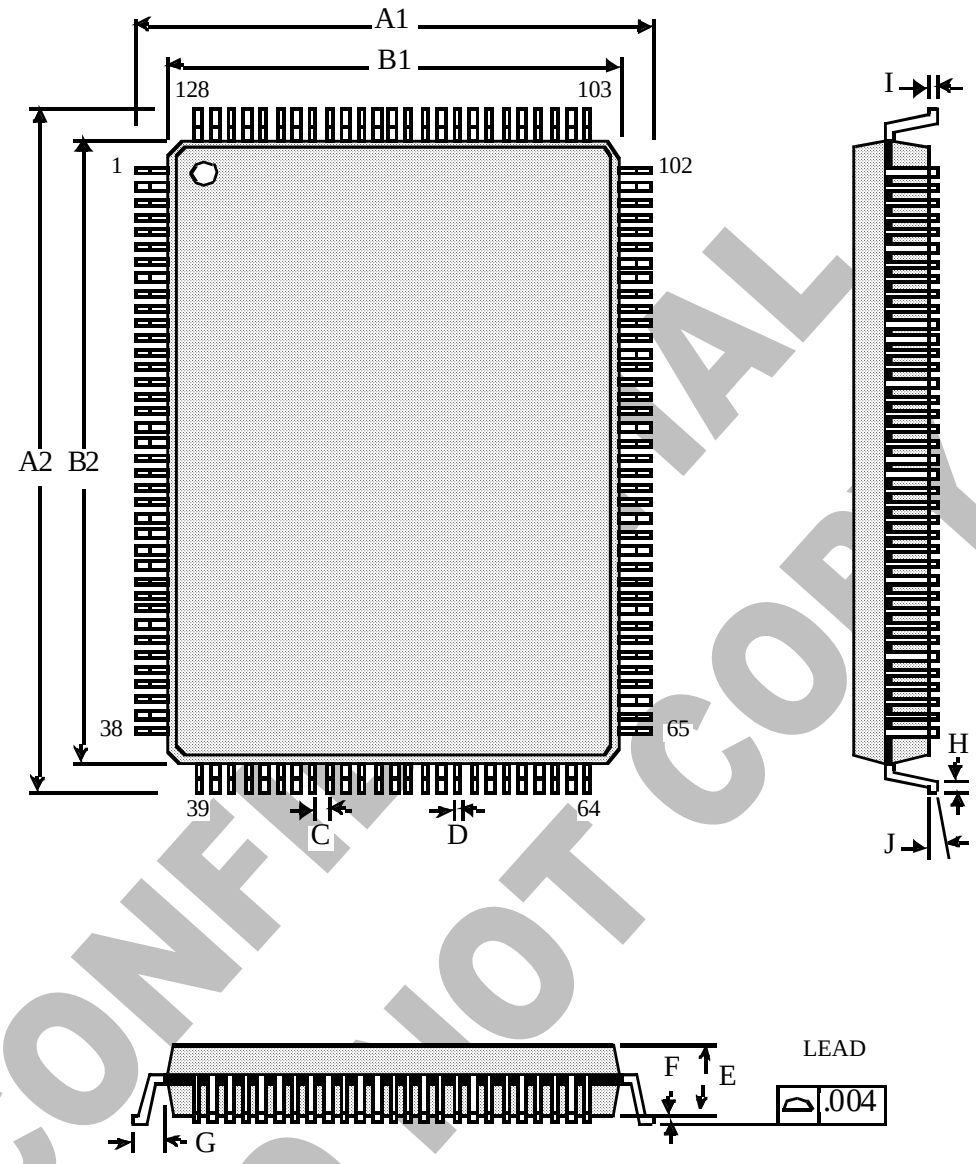

Table of Dimensions

No. of Leads		SYMBOL											
		A1	A2	B1	B2	C	D	E	F	G	H	I	J
128 (14X20)													
Milli-meters	MIN	16	22	14	20	0.50	0.17	1.35	0.05	1.00	0.45	0.09	0°
	MAX						0.27	1.45	0.15		0.75	0.20	7°

4.0 Revision History

Revision #	Date	Section	Description
0.2	3/14/2001	Package Diagram Pin Definition	Changed package from 14x14 LQFP to 14x20 LQFP.
0.3	5/02/2001	Pin Definition	Swap pin 115 and 116
0.4	5/11/2001	VREF2 definition	Set threshold for HIN, VIN, SPC, SPD, SDC & SDD

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