CH7019 TV Encoder / LVDS Transmitter

Features

TV-Out:
- VGA to TV conversion supporting up to 1024x768
- Macrovision™ 7.1.L1 copy protection support
- Two variable-voltage digital input ports.
- Simultaneous LVDS and TV output.
- True scale rendering engine supports under-scan in all TV output resolutions †¥
- Enhanced text sharpness and adaptive flicker removal with up to 7 lines of filtering ¥
- Support for NTSC and PAL TV formats
- Outputs CVBS, S-Video, RGB and YPrPb
- Support for SCART connector
- TV / Monitor connection detect
- Output video switch for easy wiring to connectors

LVDS-Out:
- Single / Dual LVDS transmitter
- Dual LVDS supports pixel rate up to 330Mpixels/sec. when both 12-bit input ports are ganged together
- LVDS low jitter PLL accepts spread spectrum input
- LVDS 18-bit output
- 2D dither engine
- Panel protection and power down sequencing
- Programmable power management

- Support for second CRT DAC bypass mode
- Four 10-bit video DAC outputs
- Fully programmable through serial port
- Complete Windows and DOS driver support
- Variable voltage interface to graphics device
- Offered in a 128-pin LQFP package

1.0 General Description

The CH7019 is a Display Controller device which accepts two digital graphics input data streams. One data stream outputs through an LVDS transmitter to an LCD panel, while the other data stream is encoded for NTSC or PAL TV and outputs through a 10-bit high speed DAC. The TV encoder device encodes a graphics signal up to 1024x768 resolution and outputs the video signals according to NTSC or PAL standards. The LVDS transmitter operates at pixel speeds up to 165MHz per link, supporting 1600x1200 panels at 60Hz refresh rate.

The device can also accept one graphics data stream over two 12-bit wide variable voltage ports which support nine different data formats including RGB and YCrCb (RGB must be used for LVDS output). A maximum of 330M pixels per second can be output through dual LVDS links.

The TV-Out processor will perform non-interlaced to interlaced conversion with scaling, flicker filtering, and encoding into any of the NTSC or PAL video standards. The scaler and flicker filter are adaptive and programmable for superior text display. Eight graphics resolutions are supported up to 1024 by 768 with full vertical and horizontal under-scan capability in all modes. A high accuracy low jitter phase locked loop is integrated to create outstanding video quality. Support is provided for Macrovision™. In addition to TV encoder modes, bypass modes are included which allow the TV DACs to be used as a second CRT DAC.

The LVDS transmitter includes a programmable dither function for support of 18-bit panels. Data is encoded into commonly used formats, including those detailed in the OpenLDI and the SPWG specifications. Serialized data outputs on three to six differential channels.

† Patent number 5,781,241
¥ Patent number 5,914,753

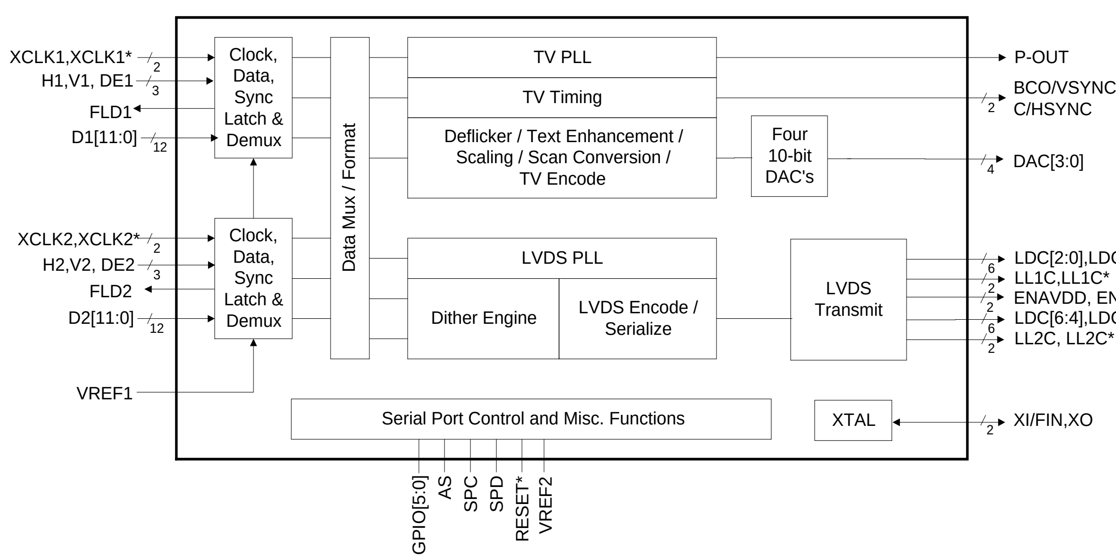

Figure 1: CH7019 Functional Block Diagram

2.0 Pin Assignment

Disclaimer: The information contained in this document is preliminary and subject to change without notice. Chrontel Inc. bears no responsibility for any errors in this document. Please contact Chrontel Inc. for design reviews prior to finalize your design.

2.1 Package Diagram

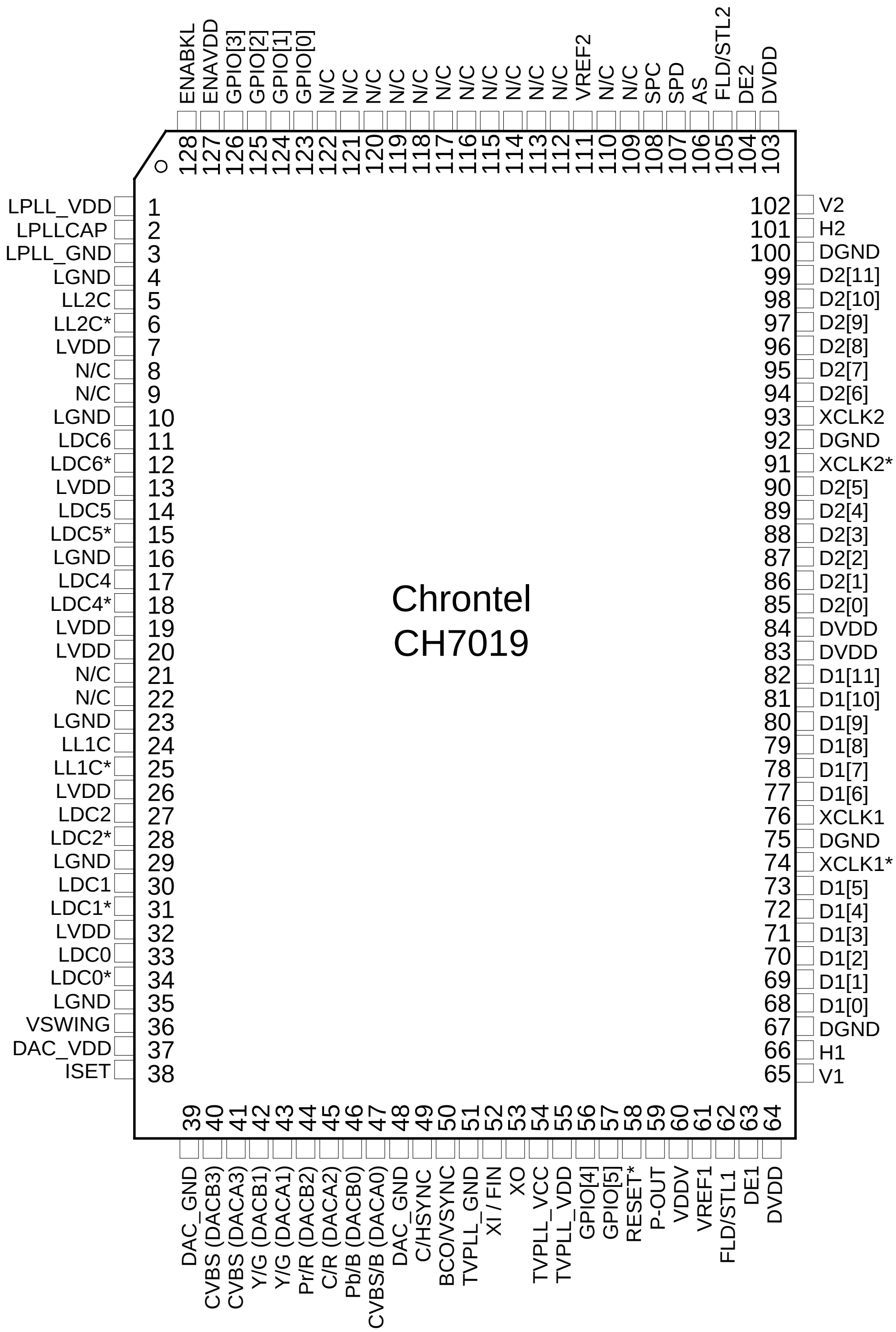

Figure 2: CH7019 128 Pin LQFP Package (Top View)

2.2 Pin Description

Table 1: Pin Description

Pin #	# of Pins	Type	Symbol	Description
66, 101	2	In/Out	H1, H2	**Horizontal Sync Input / Output** When the SYO control bit is low, these pins accept a horizontal sync inputs for use with the input data. The amplitude will be 0 to VDDV. VREF1 is the threshold level for these inputs. These pins must be used as inputs in RGB Bypass mode. When the SYO control bit is high, the TV encoder will output a horizontal sync pulse 64 pixels wide to one of these pins. The output is driven from the DVDD supply. This output is valid only when TV-Out is in operation.
65, 102	2	In/Out	V1, V2	**Vertical Sync Input / Output** When the SYO control bit is low, these pins accept a vertical sync inputs for use with the input data. The amplitude will be 0 to VDDV. VREF1 signal is the threshold level. These pins must be used as inputs in RGB Bypass mode. When the SYO control bit is high, the TV encoder will output a vertical sync pulse one line wide to one of these pins. The output is driven from the DVDD supply. This output is valid only when TV-Out is in operation.
63, 104	2	In	DE1, DE2	**Data Enable** These pins accept a data enable signal which is high when active video data is input to the device, and remains low during all other times. The levels are 0 to VDDV. VREF1 is the threshold level. The TV-Out function uses H and V sync signals and values in the SAV register as reference to active video.
62, 105	2	Out	FLD1, FLD2	**TV Field Signal** These outputs can be programmed to be a TV Field output from the TV encoder. These outputs are tri-stated upon power up.
107	1	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port and can operate with inputs from VDDV to DVDD. Outputs are driven from 0 to VREF2.
108	1	In	SPC	**Serial Port Clock Input** This pin functions as the clock input of the serial port and can operate with inputs from VDDV to DVDD.
106	1	In	AS	**Address Select** (Internal Pull-up) This pin determines the device address of the serial port.
111	1	In	VREF2	**Reference Voltage 2** Used to generate the output supply level for SPD port. This pin should be tied externally to the maximum voltage seen by the ports. (1.5V to 3.3V).
123-126, 56, 57	6	In/Out	GPIO[5:0]	**General Purpose Input / Output [5:0]** These pins provide general purpose I/O and are controlled via the serial port. (3.3V). See description of GPIO Controls for I/O configuration.
127	1	Out	ENAVDD	**Panel Power Enable** Enable panel VDD. (3.3V)
128	1	Out	ENABLK	**Back Light Enable** Enable Back-Light of LCD Panel. (3.3V)
36	1	In	VSWING	**LVDS Voltage Swing Control** This pin sets the swing level of the LVDS outputs. A 2.4K Ohm resistor should be connected between this pin and LGND (pin 35) using short and wide traces.
58	1	In	RESET*	**Reset * Input** (Internal Pull-up) When this pin is low, the device is held in the power on reset condition. When this pin is high, reset is controlled through the serial port.

Table 1: Pin Description (continued)

Pin #	# of Pins	Type	Symbol	Description
2	1	Analog	LPLLCAP	**LVDS PLL Capacitor** This pins allows coupling of any signal to the on-chip loop filter capacitor.
5, 24	2	Out	LL2C, LL1C	**Positive LVDS differential Clock2 & Clock1**
6, 25	2	Out	LL2C*, LL1C*	**Negative LVDS differential Clock2 & Clock1**
11, 14, 17	3	Out	LDC[6:4]	**Positive LVDS differential data[6:4]**
12, 15, 18	3	Out	LDC[6:4]*	**Negative LVDS differential data[6:4]**
27, 30, 33	3	Out	LDC[2:0]	**Positive LVDS differential data[2:0]**
28, 31, 34	3	Out	LDC[2:0]*	**Negative LVDS differential data [2:0]**
38	1	Analog	ISET	**Current Set Resistor Input** This pin sets the DAC current. A 140-ohm resistor should be connected between this pin and DAC_GND (pin 39) using short and wide traces.
40	1	Out	CVBS (DACB3)	**Composite Video** This pin outputs a composite video signal capable of driving a 75 ohm doubly terminated load. During bypass modes this output is valid only if the data format is compatible with one of the TV-Out display modes.
41	1	Out	CVBS (DACA3)	**Composite Video** This pin outputs a composite video signal capable of driving a 75 ohm doubly terminated load. During bypass modes this output is valid only if the data format is compatible with one of the TV-Out display modes.
42	1	Out	Y/G (DACB1)	**Luma / Green Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be the luminance component of YPrPb or green (for VGA bypass)
43	1	Out	Y/G (DACA1)	**Luma / Green Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be s-video luminance or green (for SCART type 1 connections)
44	1	Out	Pr/R (DACB2)	**Pr / Red Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be the Pr component of YPrPb or red (for VGA bypass)
45	1	Out	C/R (DACA2)	**Chroma / Red Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be s-video chrominance or red (for SCART type 1 connections)
42	1	Out	Pb/B (DACB0)	**Pb / Blue Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to the Pb component of YPrPb or blue (for VGA bypass).
43	1	Out	CVBS/B (DACA0)	**Composite Video / Blue Output** This pin outputs a selectable video signal. The output is designed to drive a 75 ohm doubly terminated load. The output can be selected to be composite video or blue (for SCART type 1 connections)
49	1	Out	C/HSYNC	**Composite / Horizontal Sync** Provides composite sync in TV modes and horizontal sync in bypass RGB mode. This pin is driven by the DVDD supply.
50	1	Out	BCO/VSYNC	**Buffered Clock Outputs / Vertical Sync** This output pin provides buffered crystal oscillator clock output or VSYNC output in bypass RGB mode. This pin is driven by the DVDD supply.
52	1	In	XI / FIN	**Crystal Input / External Reference Input** A parallel resonant 14.31818MHz crystal ($\pm$ 20 ppm) should be attached between this pin and XO. However, an external CMOS compatible clock can drive the XI/FIN input.

Table 1: Pin Description (continued)

Pin #	# of Pins	Type	Symbol	Description
53	1	Out	XO	**Crystal Output** A parallel resonance 14.31818MHz crystal (± 20 ppm) should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open.
59	1	Out	P-Out	**Pixel Clock Output** This pin provides a pixel clock signal to the VGA controller which can be used as a reference frequency. The output is selectable between 1X and 2X of the pixel clock frequency. The output driver is driven from the VDDV supply (pin 60). This output has a programmable tri-state. The capacitive loading on this pin should be kept to a minimum.
61	1	In	VREF1	**Reference Voltage Input 1** The VREF1 pin inputs a reference voltage of VDDV / 2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, sync and clock inputs.
68-73, 77-82	12	In	D1[11:0]	**Data1[11] through Data1[0] Inputs** These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to VDDV. VREF1 is the threshold level.
76, 74	2	In	XCLK1, XCLK1*	**External Clock Inputs** These inputs form a differential clock signal input to the device for use with the H1, V1 and D1[11:0] data. If differential clocks are not available, the XCLK1* input should be connected to VREF1. The clock polarity can be selected by the MCP1 control bit.
85-90, 94-99	12	In	D2[11:0]	**Data2[11] through Data2[0] Inputs** These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to VDDV. VREF1 is the threshold level.
93, 91	2	In	XCLK2, XCLK2*	**External Clock Inputs** These inputs form a differential clock signal input to the device for use with the H2, V2 and D2[11:0] data. If differential clocks are not available, the XCLK2* input should be connected to VREF1. The clock polarity can be selected by the MCP2 control bit.
64, 83, 84, 103	4	Power	DVDD	**Digital Supply Voltage** (3.3V)
67, 75, 92, 100	4	Power	DGND	**Digital Ground**
60	1	Power	VDDV	**I/O Supply Voltage** (1.1V to 3.3V)
55	2	Power	TVPLL_VDD	**TV PLL Supply Voltage** (3.3V)
54	1	Power	TVPLL_VCC	**TV PLL Supply Voltage** (3.3V)
51	1	Power	TVPLL_GND	**TV PLL Ground**
37	1	Power	DAC_VDD	**DAC Supply Voltage** (3.3V)
39, 48	1	Power	DAC_GND	**DAC Ground**
7, 13, 19, 20, 26, 32	6	Power	LVDD	**LVDS Supply Voltage** (3.3V)
4, 10, 16, 23, 29, 35	6	Power	LGND	**LVDS Ground**
1	1	Power	LPLL_VDD	**LVDS PLL Supply Voltage** (3.3V)
3	1	Power	LPLL_GND	**LVDS PLL Ground**
8, 9, 21, 22, 109, 110, 112-122	13		N/C	**Not Connected**

3.0 Overview

The CH7019 is a VGA to TV encoder with dual LVDS output for the graphics subsystem. Both TV-Out and LVDS-Out can operate simultaneously if the two 12-bit input ports are driven from different timing generators. TV timing requirements are usually different from that of the TFT-LCD panels. If the graphic controller can generate only one set of timing, simultaneous display on both the TV and the flat panel may not be available for all graphic modes. Descriptions of each of the operating modes with block diagrams of the data flow within the device are shown below.

The CH7019 also supports 24-bit input mode by ganging D1 and D2 together as a single 24-bit data port. In this case the timing signals H1, V1, DE1, XCLK1 and XCLK1* are equal to H2, V2, DE2, XCLK2 and XCL2* , respectively. Video data are sent to either the TV encoder (including RGB bypass) or to the LVDS data path, but not both. Maximum data rate supported through the dual LVDS links is 330M Pixels /sec. The maximum pixel rate supported by the RGB bypass mode is 165 Mpixels/sec.

3.1 Input Interface Timing

Four distinct methods of transferring data to the CH7019 are described below. In each of the four modes, DEx is used to signal active LVDS data for the panel and register SAV value denotes the start of active TV video.

A. 12-bit Multiplexed Data – Dual-edge Transfer

- Multiplexed data - two 12-bit words per pixel from either D1[11:0] or D2[11:0]
- Clock frequency equals 1X pixel rate with 12-bit data transfer at both rising and falling clock edges.
- Maximum pixel rate is 165M pixels per second with a 165 MHz pixel clock.
- Simultaneous TV and panel display.

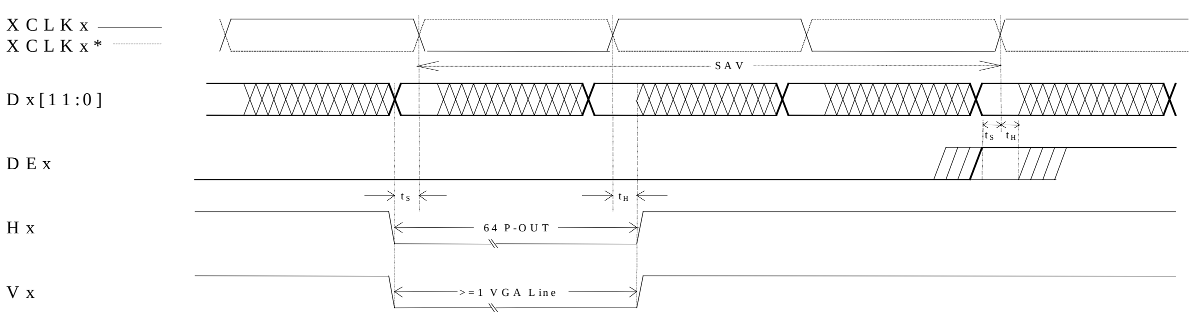

Figure 3: Interface Timing for Multiplexed Data – Dual-edge Transfer

B. 12-bit Multiplexed Data – Single-edge Transfer

- Multiplexed data - two 12-bit words per pixel from either D1[11:0] or D2[11:0]
- Clock frequency equals 2X pixel rate with 12-bit data transfer at either rising or falling edge of clock (programmable via serial port).
- Maximum pixel rate is 165M pixels per second with a 330 MHz pixel clock.
- Simultaneous TV and panel display.

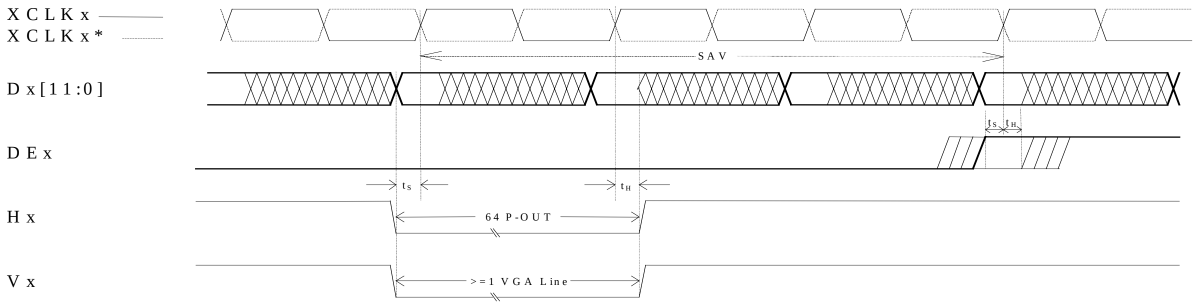

Figure 4: Interface Timing for Multiplexed Data – Single-edge Transfer

C. 24-bit Ganged Data – Dual-edge Transfer

- Multiplexed data - two 24-bit words per pixel from both D1[11:0] and D2[11:0]
- Clock frequency equals 1/2X pixel rate with 24-bit data transfer at both rising and falling clock edges.
- Maximum pixel rate is 330M pixels per second with a 165 MHz pixel clock.
- No Simultaneous TV and panel display.

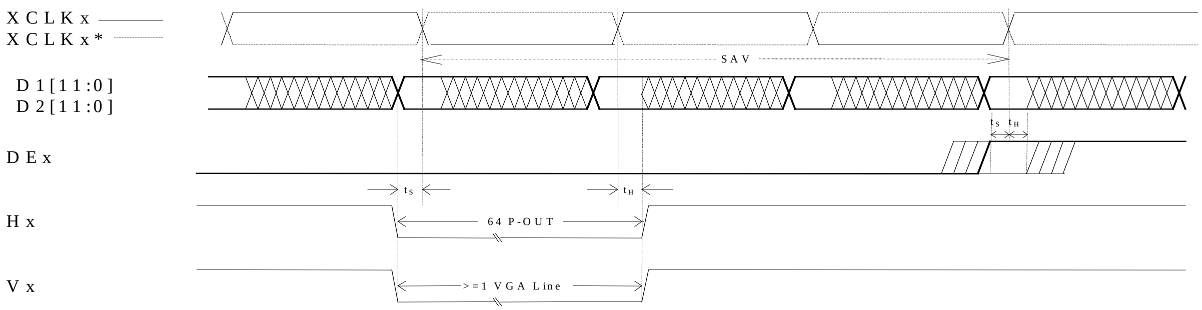

Figure 5: Interface Timing for 24-bit Multiplexed Data – Dual-edge Transfer

D. 24-bit Ganged Data – Single-edge Transfer

- Non-multiplexed data - one 24-bit word per pixel from both D1[11:0] and D2[11:0].
- Clock frequency equals 1X pixel rate with 24-bit data transfer at either rising or falling edge of clock (programmable via serial port).
- Maximum pixel rate is 330M pixels per second with a 330 MHz pixel clock.
- No simultaneous TV and panel display.

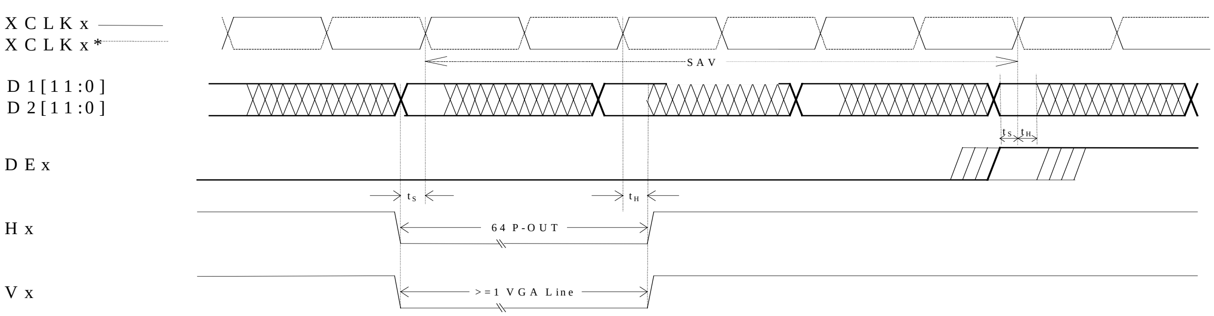

Figure 6: Interface Timing for Non-multiplexed Data – Single-edge Transfer

Table 2: Interface Timing Specifications

Symbol	Parameter	Min	Typ	Max	Unit
t_S	Setup time	See section 5.5			nS
t_H	Hold time	See section 5.5			nS

Note: t_S, t_H, setup time and hold time are programmable through serial port – X1CMD [3:0] and X2CMD[3:0] by delay or advance of clock relative to data.

3.2 Input Data Formats

3.2.1 12-Bit Multiplexed Data Formats

Multiplexed pixel data inputs to the CH7019 through D1[11:0] or D2[11:0] using data transfer method A or B described in 3.1. Received data is formatted and sent through an internal data bus P1[23:0] to TV encoder or directly to the TV DACs, or through bus P2[23:0] to the LVDS data path. The multiplexed input data formats are (IDF1[3:0]=0,1,2,3 and 4 for D1 and IDF2[3:0]=0,1,2,3 and 4 for D2):

IDFx	Description
0	RGB 8-8-8 (2x12-bit)
1	RGB 8-8-8 (2x12-bit) or RGB 5-6-5 (2x8-bit)
2	RGB 5-6-5 (2x8bit)
3	RGB 5-5-5 (2x8-bit)
4	YCrCb 8-8 (2x8-bit)

For multiplexed input data formats, data can be latched from the graphics controller by either rising only or falling only clock edges, or by both rising and falling clock edges. The MCPx bits select the rising or the falling clock edge, where rising refers to rising edge on the XCLKx signals and falling edge on the XCLKx* signals. The multiplexed input data formats are shown in Figure 7 below. The input data bus Dx[11:0], where x can be either 1 or 2, transports a 12-bit or 8-bit multiplexed data stream containing either RGB or YcrCb formatted data. The input data rate is 2X the pixel rate and each pair of Pn values (e.g.; P0a and P0b) contains a complete pixel encoded as shown in the Tables 3 to 6 below and can be placed onto one or both of the internal pixel buses Py[23:0], where y equals 1 or 2. It is assumed that the first clock cycle following the leading edge of the incoming horizontal sync signal contains the first word (Pxa) of a pixel, if an active pixel was present immediately following the horizontal sync. When the input is a YCrCb data stream the color-difference data will be transmitted at half the data rate of the luminance data with the sequence being set as Cb0, Y0, Cr0, Y1, where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples and the following Y1 byte refers to the next luminance sample, per CCIR-656 standards (the clock frequency is dependent upon the current mode, and is not 27MHz as specified in CCIR-656). All non-active pixels should be 0 in RGB formats, and 16 for Y and 128 for CrCb in YCrCb formats.

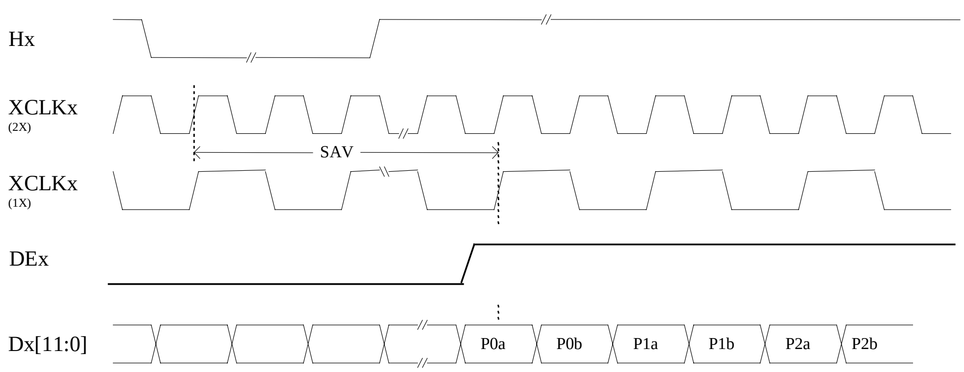

Figure 7: 12-bit Multiplexed Input Data Formats (IDFx = 0,1,2,3,4)

Table 3: Multiplexed Input Data Formats (IDFx = 0, 1)

IDFx = Format =		**0 RGB 8-8-8 (2x12-bit) For TV/Bypass RGB or/and LVDS**				**1 RGB 8-8-8 (2x12-bit) or RGB 5-6-5 (2x8-bit) For TV/Bypass RGB or/and LVDS**			
Pixel #		P0a	P0b	P1a	P1b	P0a	P0b	P1a	P1b
Bus Data	Dx[11]	G0[3]	R0[7]	G1[3]	R1[7]	G0[4]	R0[7]	G1[4]	R1[7]
	Dx[10]	G0[2]	R0[6]	G1[2]	R1[6]	G0[3]	R0[6]	G1[3]	R1[6]
	Dx[9]	G0[1]	R0[5]	G1[1]	R1[5]	G0[2]	R0[5]	G1[2]	R1[5]
	Dx[8]	G0[0]	R0[4]	G1[0]	R1[4]	B0[7]	R0[4]	B1[7]	R1[4]
	Dx[7]	B0[7]	R0[3]	B1[7]	R1[3]	B0[6]	R0[3]	B1[6]	R1[3]
	Dx[6]	B0[6]	R0[2]	B1[6]	R1[2]	B0[5]	G0[7]	B1[5]	G1[7]
	Dx[5]	B0[5]	R0[1]	B1[5]	R1[1]	B0[4]	G0[6]	B1[4]	G1[6]
	Dx[4]	B0[4]	R0[0]	B1[4]	R1[0]	B0[3]	G0[5]	B1[3]	G1[5]
	Dx[3]	B0[3]	G0[7]	B1[3]	G1[7]	G0[0]	R0[2]	G1[0]	R1[2]
	Dx[2]	B0[2]	G0[6]	B1[2]	G1[6]	B0[2]	R0[1]	B1[2]	R1[1]
	Dx[1]	B0[1]	G0[5]	B1[1]	G1[5]	B0[1]	R0[0]	B1[1]	R1[0]
	Dx[0]	B0[0]	G0[4]	B1[0]	G1[4]	B0[0]	G0[1]	B1[0]	G1[1]

Table 4: Multiplexed Input Data Formats (IDFx = 2, 3)

IDFx = Format =		**2 RGB 5-6-5 (2x8bit) for TV/Bypass RGB or/and LVDS**				**3 RGB 5-5-5 (2x8-bit) for TV/Bypass RGB or/and LVDS**			
Pixel #		P0a	P0b	P1a	P1b	P0a	P0b	P1a	P1b
Bus Data	Dx[11]	G0[4]	R0[7]	G1[4]	R1[7]	G0[5]	X	G1[5]	X
	Dx[10]	G0[3]	R0[6]	G1[3]	R1[6]	G0[4]	R0[7]	G1[4]	R1[7]
	Dx[9]	G0[2]	R0[5]	G1[2]	R1[5]	G0[3]	R0[6]	G1[3]	R1[6]
	Dx[8]	B0[7]	R0[4]	B1[7]	R1[4]	B0[7]	R0[5]	B1[7]	R1[5]
	Dx[7]	B0[6]	R0[3]	B1[6]	R1[3]	B0[6]	R0[4]	B1[6]	R1[4]
	Dx[6]	B0[5]	G0[7]	B1[5]	G1[7]	B0[5]	R0[3]	B1[5]	R1[3]
	Dx[5]	B0[4]	G0[6]	B1[4]	G1[6]	B0[4]	G0[7]	B1[4]	G1[7]
	Dx[4]	B0[3]	G0[5]	B1[3]	G1[5]	B0[3]	G0[6]	B1[3]	G1[6]

Table 5: Multiplexed Input Data Formats (IDFx = 4)

IDFx = Format =		**4 YCrCb 4:2:2 (2x8-bit) for TV**							
Pixel #		P0a	P0b	P1a	P1b	P2a	P2b	P3a	P3b
Bus Data	Dx[7]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	Dx[6]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	Dx[5]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	Dx[4]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	Dx[3]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	Dx[2]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	Dx[1]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	Dx[0]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

When IDFx = 4 (YCrCb mode), the data inputs can also be used to transmit sync information to the device. In this mode, the embedded sync will follow the VIP2 convention, and the first byte of the 'video timing reference code' will be assumed to occur when a Cb sample would occur, if the video stream was continuous. This is shown below:

Table 6: Multiplexed Input Data Formats (IDFx = 4) with Embedded Sync

IDFx = Format =		4 YCrCb 4:2:2 (2x8-bit) for TV							
Pixel #		P0a	P0b	P1a	P1b	P2a	P2b	P3a	P3b
Bus Data	Dx[7]	1	0	0	S[7]	Cb2[7]	Y2[7]	Cr2[7]	Y3[7]
	Dx[6]	1	0	0	S[6]	Cb2[6]	Y2[6]	Cr2[6]	Y3[6]
	Dx[5]	1	0	0	S[5]	Cb2[5]	Y2[5]	Cr2[5]	Y3[5]
	Dx[4]	1	0	0	S[4]	Cb2[4]	Y2[4]	Cr2[4]	Y3[4]
	Dx[3]	1	0	0	S[3]	Cb2[3]	Y2[3]	Cr2[3]	Y3[3]
	Dx[2]	1	0	0	S[2]	Cb2[2]	Y2[2]	Cr2[2]	Y3[2]
	Dx[1]	1	0	0	S[1]	Cb2[1]	Y2[1]	Cr2[1]	Y3[1]
	Dx[0]	1	0	0	S[0]	Cb2[0]	Y2[0]	Cr2[0]	Y3[0]

In this mode, the S[7..0] byte contains the following data:
S[6] = F = 1 during field 2, 0 during field 1
S[5] = V = 1 during field blanking, 0 elsewhere
S[4] = H = 1 during EAV (synchronization reference at the end of active video)
0 during SAV (synchronization reference at the start of active video)
S[7] and S[3:0] are ignored

3.2.2 24-Bit Data Formats

The two 12-bit input data ports, D1[11:0] and D2[11:0], can be grouped together to form a single 24-bit interface to the graphic controller. In this case the timing signals H1, V1, DE1, XCLK1 and XCLK1* are equal to H2, V2, DE2, XCLK2 and XCL2* , respectively. The CH7019 supports 5 different 24-bit data formats. Each of which is used with a 1X pixel rate clock latching data with one of the clock edges (default is falling edge). The 24-bit input data formats are IDFx[3:0]=5,6,7,8 and 9 (note that IDF1 must be set equal to IDF2) and are illustrated in Figure 8 below.

IDFx	Description
5	RGB 8-8-8 (1x24-bit) for TV/Bypass RGB
6	YCrCb 8-8 (1x16-bit with CrCb multiplexed and decimated by 2) for TV
7	YCrCb 8-8-8 (1x24-bit) for TV
8	RGB 8-8-8 (2x24-bit) Odd / Even Ganged for LVDS
9	RGB 8-8-8 (1x24-bit) Normal Ganged for LVDS

The pixel data bus represents a 24-bit or 16-bit data stream containing either RGB or YCrCb formatted data. When the input is a 16-bit YCrCb data stream the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb0, Y0 transmitted during one clock cycle, followed by Cr0, Y1 the following clock cycle, where Cb0, Y0, Cr0 refers to co-sited luminance and color-difference samples and the Y1 data refers to the next luminance sample, per CCIR-601 sampling. Non-active data must be 0 in RGB format, and 16 for Y, 128 for Cr and Cb in YCrCb formats.

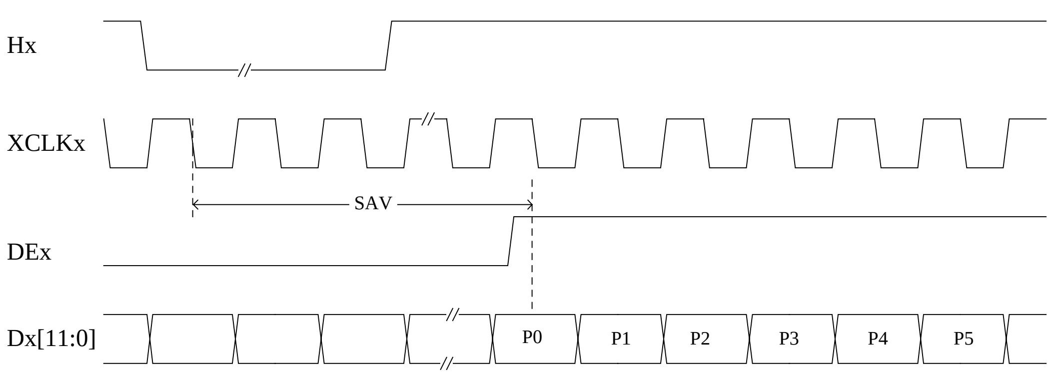

Figure 8: Non-Multiplexed Input Data Formats (IDFx = 5,6,7,8 and 9)

Table 7: Non-Multiplexed Data Formats

IDFx = Format =		5 24-bit RGB for TV/Bypass RGB		6 16-bit YCrCb FOR TV				7 24-bit YCrCb FOR TV	
Pixel #		**P0**	**P1**	**P0**	**P1**	**P2**	**P3**	**P0**	**P1**
Bus Data	D1[11]	R0[7]	R1[7]	Y0[7]	Y1[7]	Y2[7]	Y3[7]	Y0[7]	Y1[7]
	D1[10]	R0[6]	R1[6]	Y0[6]	Y1[6]	Y2[6]	Y3[6]	Y0[6]	Y1[6]
	D1[9]	R0[5]	R1[5]	Y0[5]	Y1[5]	Y2[5]	Y3[5]	Y0[5]	Y1[5]
	D1[8]	R0[4]	R1[4]	Y0[4]	Y1[4]	Y2[4]	Y3[4]	Y0[4]	Y1[4]
	D1[7]	R0[3]	R1[3]	Y0[3]	Y1[3]	Y2[3]	Y3[3]	Y0[3]	Y1[3]
DVOB	D1[6]	R0[2]	R1[2]	Y0[2]	Y1[2]	Y2[2]	Y3[2]	Y0[2]	Y1[2]
	D1[5]	R0[1]	R1[1]	Y0[1]	Y1[1]	Y2[1]	Y3[1]	Y0[1]	Y1[1]
	D1[4]	R0[0]	R1[0]	Y0[0]	Y1[0]	Y2[0]	Y3[0]	Y0[0]	Y1[0]
	D1[3]	G0[7]	G1[7]	Cr0[7]	Cb0[7]	Cr2[7]	Cb2[7]	Cr0[7]	Cr1[7]
	D1[2]	G0[6]	G1[6]	Cr0[6]	Cb0[6]	Cr2[6]	Cb2[6]	Cr0[6]	Cr1[6]
	D1[1]	G0[5]	G1[5]	Cr0 [5]	Cb0 [5]	Cr2 [5]	Cb2 [5]	Cr0 [5]	Cr1 [5]
	D1[0]	G0[4]	G1[4]	Cr0 [4]	Cb0 [4]	Cr2 [4]	Cb2 [4]	Cr0 [4]	Cr1 [4]
	D2[11]	G0[3]	G1[3]	Cr0 [3]	Cb0 [3]	Cr2 [3]	Cb2 [3]	Cr0 [3]	Cr1 [3]
	D2[10]	G0[2]	G1[2]	Cr0 [2]	Cb0 [2]	Cr2 [2]	Cb2 [2]	Cr0 [2]	Cr1 [2]
	D2[9]	G0[1]	G1[1]	Cr0 [1]	Cb0 [1]	Cr2 [1]	Cb2 [1]	Cr0 [1]	Cr1 [1]
	D2[8]	G0[0]	G1[0]	Cr0 [0]	Cb0 [0]	Cr2 [0]	Cb2 [0]	Cr0 [0]	Cr1 [0]
	D2[7]	B0[7]	B1[7]					Cb0[7]	Cb1[7]
DVOC	D2[6]	B0[6]	B1[6]					Cb0[6]	Cb1[6]
	D2[5]	B0[5]	B1[5]					Cb0 [5]	Cb1[5]
	D2[4]	B0[4]	B1[4]					Cb0 [4]	Cb1[4]
	D2[3]	B0[3]	B1[3]					Cb0 [3]	Cb1[3]
	D2[2]	B0[2]	B1[2]					Cb0 [2]	Cb1[2]
	D2[1]	B0[1]	B1[1]					Cb0 [1]	Cb1[1]
	D2[0]	B0[0]	B1[0]					Cb0 [0]	Cb1[0]

When IDFx = 6 or 7 (YCrCb modes), the data inputs can be used to transmit sync information to the device. In these modes the embedded sync follows a subset of the VIP2 convention, and the first byte of the video timing reference code is assumed to occur when a Cb sample occurs, if the video stream is continuous. This is shown in Table 8 below.

Table 8: Non-Multiplexed YCrCb modes with Embedded Sync

IDFx = **Format =**		**6** **16-bit YCrCb** **for TV**				**7** **24-bit YCrCb** **for TV**			
Pixel #		**P0**	**P1**	**P2**	**P3**	**P0**	**P1**	**P2**	**P3**
Bus Data	D1[11]	0	S[7]	Y0[7]	Y1[7]	0	S[7]	Y0[7]	Y1[7]
	D1[10]	0	S[6]	Y0[6]	Y1[6]	0	S[6]	Y0[6]	Y1[6]
	D1[9]	0	S[5]	Y0[5]	Y1[5]	0	S[5]	Y0[5]	Y1[5]
	D1[8]	0	S[4]	Y0[4]	Y1[4]	0	S[4]	Y0[4]	Y1[4]
	D1[7]	0	S[3]	Y0[3]	Y1[3]	0	S[3]	Y0[3]	Y1[3]
	D1[6]	0	S[2]	Y0[2]	Y1[2]	0	S[2]	Y0[2]	Y1[2]
	D1[5]	0	S[1]	Y0[1]	Y1[1]	0	S[1]	Y0[1]	Y1[1]
	D1[4]	0	S[0]	Y0[0]	Y1[0]	0	S[0]	Y0[0]	Y1[0]
	D1[3]	1	0	Cr0[7]	Cb0[7]	1	X	Cr0[7]	Cr1[7]
	D1[2]	1	0	Cr0[6]	Cb0[6]	1	X	Cr0[6]	Cr1[6]
	D1[1]	1	0	Cr0 [5]	Cb0 [5]	1	X	Cr0 [5]	Cr1[5]
	D1[0]	1	0	Cr0 [4]	Cb0 [4]	1	X	Cr0 [4]	Cr1[4]
	D2[11]	1	0	Cr0 [3]	Cb0 [3]	1	X	Cr0 [3]	Cr1[3]
	D2[10]	1	0	Cr0 [2]	Cb0 [2]	1	X	Cr0 [2]	Cr1[2]
	D2[9]	1	0	Cr0 [1]	Cb0 [1]	1	X	Cr0 [1]	Cr1[1]
	D2[8]	1	0	Cr0 [0]	Cb0 [0]	1	X	Cr0 [0]	Cr1[0]
	D2[7]					0	X	Cb0[7]	Cb1[7]
	D2[6]					0	X	Cb0[6]	Cb1[6]
	D2[5]					0	X	Cb0 [5]	Cb1 [5]
	D2[4]					0	X	Cb0 [4]	Cb1 [4]
	D2[3]					0	X	Cb0 [3]	Cb1 [3]
	D2[2]					0	X	Cb0 [2]	Cb1 [2]
	D2[1]					0	X	Cb0 [1]	Cb1 [1]
	D2[0]					0	X	Cb0 [0]	Cb1 [0]

In this mode, the S[7..0] byte contains the following data:
S[6] = F = 1 during field 2, 0 during field 1
S[5] = V = 1 during field blanking, 0 elsewhere
S[4] = H = 1 during EAV (synchronization reference at the end of active video)
0 during SAV (synchronization reference at the start of active video)
S[7] and S[3:0] are ignored

Under mode 8 and 9, the CH7019 takes 24-bit data from both D1 and D2 and outputs to the dual LVDS links. A maximum throughput of 330M pixels per second can be achieved. The timing signals of both input ports shall be identical. H1, V1 and XCLK1 equal H2, V2 and XCLK2, respectively. Up-scaling and dithering functions are not available in these modes.

Table 9: Ganged Data Formats

IDFx = Format =		**8 24-bit RGB Odd/Even Ganged for LVDS**		**9 24-bit RGB Normal Ganged for LVDS**	
Pixel #		**P0**	**P1**	**P0**	**P1**
Bus Data	D1[11]	G0[3]	R0[7]	R0[7]	R1[7]
	D1[10]	G0[2]	R0[6]	R0[6]	R1[6]
	D1[9]	G0[1]	R0[5]	R0[5]	R1[5]
	D1[8]	G0[0]	R0[4]	R0[4]	R1[4]
	D1[7]	B0[7]	R0[3]	R0[3]	R1[3]
DVOB	D1[6]	B0[6]	R0[2]	R0[2]	R1[2]
	D1[5]	B0[5]	R0[1]	R0[1]	R1[1]
	D1[4]	B0[4]	R0[0]	R0[0]	R1[0]
	D1[3]	B0[3]	G0[7]	G0[7]	G1[7]
	D1[2]	B0[2]	G0[6]	G0[6]	G1[6]
	D1[1]	B0[1]	G0[5]	G0[5]	G1[5]
	D1[0]	B0[0]	G0[4]	G0[4]	G1[4]
	D2[11]	G1[3]	R1[7]	G0[3]	G1[3]
	D2[10]	G1[2]	R1[6]	G0[2]	G1[2]
	D2[9]	G1[1]	R1[5]	G0[1]	G1[1]
	D2[8]	G1[0]	R1[4]	G0[0]	G1[0]
	D2[7]	B1[7]	R1[3]	B0[7]	B1[7]
DVOC	D2[6]	B1[6]	R1[2]	B0[6]	B1[6]
	D2[5]	B1[5]	R1[1]	B0[5]	B1[5]
	D2[4]	B1[4]	R1[0]	B0[4]	B1[4]
	D2[3]	B1[3]	G1[7]	B0[3]	B1[3]
	D2[2]	B1[2]	G1[6]	B0[2]	B1[2]
	D2[1]	B1[1]	G1[5]	B0[1]	B1[1]
	D2[0]	B1[0]	G1[4]	B0[0]	B1[0]

3.3 TV-Out

Multiplexed input data, sync and clock signals from the graphics controller inputs to the CH7019 through one of the two 12-bit variable voltage input ports, D1[11:0] or D2[11:0], and is directed to the TV data path. Non-multiplexed 24-bit input data also inputs through both of the two input ports. Detailed descriptions of the eight input data formats are given in Section 3.2. Clock signal (P-Out) outputs as a frequency reference to the graphics controller to ensure accurate frequency generation. Horizontal and vertical sync signals are normally sent to the CH7019 from the graphics controller, but can be optionally generated by the CH7019 and output to the graphics controller. Using the serial port, the CH7019 can be programmed as the clock master, clock slave, sync master or sync slave. Data will be 2X multiplexed (2x12 bits) or non-multiplexed (1x24 bits), and the XCLK clock signal can be 1X or 2X times the pixel rate. The input data will be encoded into the selected video standard, and output from the video DACs.

3.3.1 Display Modes

The CH7019 display mode is controlled by three independent factors: input resolution, TV format, and scale factor, which are programmed via the display mode register. It is designed to accept input resolutions of 512x384, 640x480, 640x400, 720x400, 720x480, 720x576, 800x600, and 1024x768.

It is designed to support output to either NTSC or PAL television formats. The CH7019 provides interpolated scaling with selectable factors of 5:4, 1:1, 7:8, 5:6, 3:4, 7:10 and 25:21 in order to support adjustable overscan or underscan operation when displayed on a TV. The modes supported for TV-Out are shown in the Table 10 below.

Table 10: TV Output Modes

Graphics Resolution	Active Aspect Ratio	Pixel Aspect Ratio	TV Output Standard	Scaling Ratios
512x384	4:3	1:1	PAL	5/4, 1/1
512x384	4:3	1:1	NTSC	5/4, 1/1
720x400	4:3	1.35:1.00	PAL	5/4, 1/1
720x400	4:3	1.35:1.00	NTSC	5/4, 1/1, 25/21
640x400	8:5	1:1	PAL	5/4, 1/1
640x400	8:5	1:1	NTSC	5/4, 1/1, 7/8, 25/21
640x480	4:3	1:1	PAL	5/4, 1/1, 5/6, 25/21
640x480	4:3	1:1	NTSC	1/1, 7/8, 5/6
720x480[1]	4:3	9:8	NTSC	1/1
720x480[2]	4:3	9:8	NTSC	1/1, 7/8, 5/6
720x576[1]	4:3	15:12	PAL	1/1
720x576[2]	4:3	15:12	PAL	1/1, 5/6, 5/7
800x600	4:3	1:1	PAL	1/1, 5/6, 5/7
800x600	4:3	1:1	NTSC	3/4, 7/10, 5/8
1024x768	4:3	1:1	PAL	5/7, 5/8, 5/9
1024x768	4:3	1:1	NTSC	5/8, 5/9, 1/2

[1] These DVD modes operate with interlaced input. Scan conversion and flicker filter are bypassed.
[2] These DVD modes operate with non-interlaced input. Scan conversion and flicker filter are not bypassed.

3.3.2 Adaptive Flicker Filter

The CH7019 integrates an advanced 2-line, 3-line, 4-line, 5-line, 6-line and 7-line (depending on mode) vertical deflickering filter circuit to help eliminate the flicker associated with interlaced displays. This flicker circuit provides an adaptive filter algorithm for implementing flicker reduction with selections of high, medium or low flicker content for both luma and chroma channels (see register descriptions). In addition, a special text enhancement circuit incorporates additional filtering for enhancing the readability of test. These modes are fully programmable via serial port interface using the flicker filter register.

3.3.3 Color Burst Generation

The CH7019 allows the subcarrier frequency to be accurately generated from a 14.31818 MHz crystal oscillator, leaving the subcarrier frequency independent of the graphics pixel clock frequency. As a result, the CH7019 may be used with most VGA chips (with an appropriate digital interface) since the CH7019 subcarrier frequency can be generated without being dependent on the precise pixel rates of VGA controllers. This feature is important since even a ±0.01% subcarrier frequency variation is enough to cause some televisions to lose color lock.

In addition, the CH7019 has the capability to genlock the color burst signal to the VGA horizontal sync frequency, which enables a fully synchronous system between the graphics controller and the television. When genlocked, the CH7019 can stop “dot crawl” motion (for composite NTSC modes), thus eliminating the annoyance of moving borders. Both of these features are under programmable control through the register set.

3.3.4 NTSC and PAL Operation

Composite and S-Video outputs are supported in either NTSC or PAL format. The general parameters used to characterize these outputs are listed in Table 11 and shown in Figure 9. (See Figure 12 through Figure 17 for illustrations of composite and S-Video output waveforms).

ITU-R BT.470 Compliance

The CH7019 is predominantly compliant with the recommendations called out in ITU-R BT.470. The following are the only exceptions to this compliance:

- The frequencies of Fsc, Fh, and Fv can only be guaranteed in clock/sync master mode, not in clock/sync slave mode when the graphics device generates these frequencies.
- It is assumed that gamma correction, if required, is performed in the graphics device which establishes the color reference signals.
- All modes provide the exact number of lines called out for NTSC and PAL modes respectively, except mode 21, which outputs 800x600 resolution, scaled by 3:4, to PAL format with a total of 627 lines (vs. 625).
- Chroma signal frequency response will fall within 10% of the exact recommended value.
- Pulse widths and rise/fall times for sync pulses, front/back porches, and equalizing pulses are designed to approximate ITU-R BT.470 requirements, but will fall into a range of values due to the variety of clock frequencies used to support multiple operating modes.

Table 11: NTSC/PAL Composite Output Timing Parameters

Symbol	Description	Level (mV)		Duration (uS)	
		NTSC	PAL	NTSC	PAL
A	Front Porch	287	300	1.49 - 1.51	1.48 - 1.51
B	Horizontal Sync	0	0	4.69 - 4.72	4.69 - 4.71
C	Breezeway	287	300	0.59 - 0.61	0.88 - 0.92
D	Color Burst	287	300	2.50 - 2.53	2.24 - 2.26
E	Back Porch	287	300	1.55 - 1.61	2.62 - 2.71
F	Black	340	300	0.00 - 7.50	0.00 - 8.67
G	Active Video	340	300	37.66 - 52.67	34.68 - 52.01
H	Black	340	300	0.00 - 7.50	0.00 - 8.67

For this table and all subsequent figures, key values are:

Note:

1. RSET = 140 ohms; V(ISET) = 1.235V; 75 ohms doubly terminated load. RSET is the resistor connected to the ISET pin.
2. Durations vary slightly in different modes due to the different clock frequencies used.
3. Active video and black (F, G, H) times vary greatly due to different scaling ratios used in different modes.
4. Black times (F and H) vary with position controls.

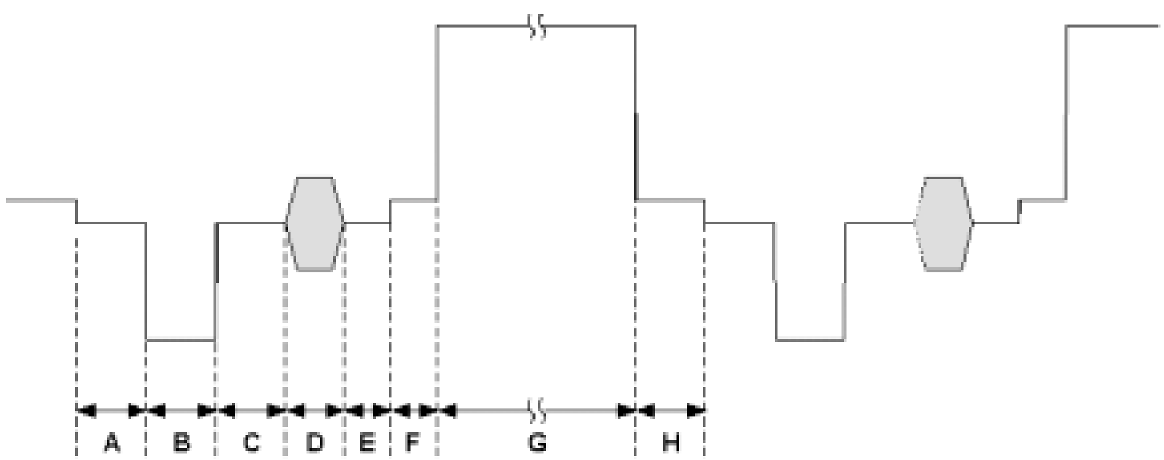

Figure 9: NTSC / PAL Composite Output

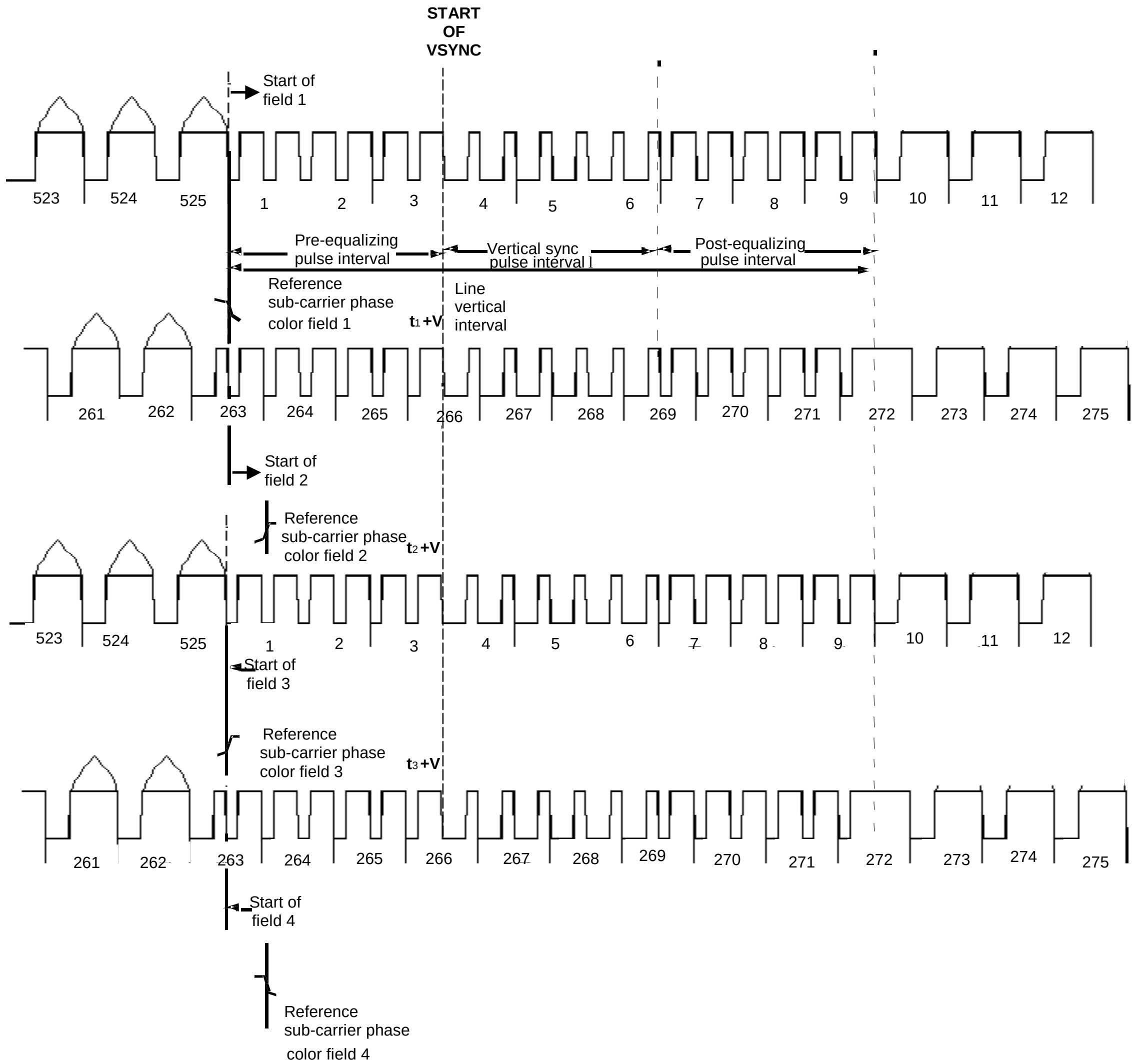

Figure 10: Interlaced NTSC Video Timing

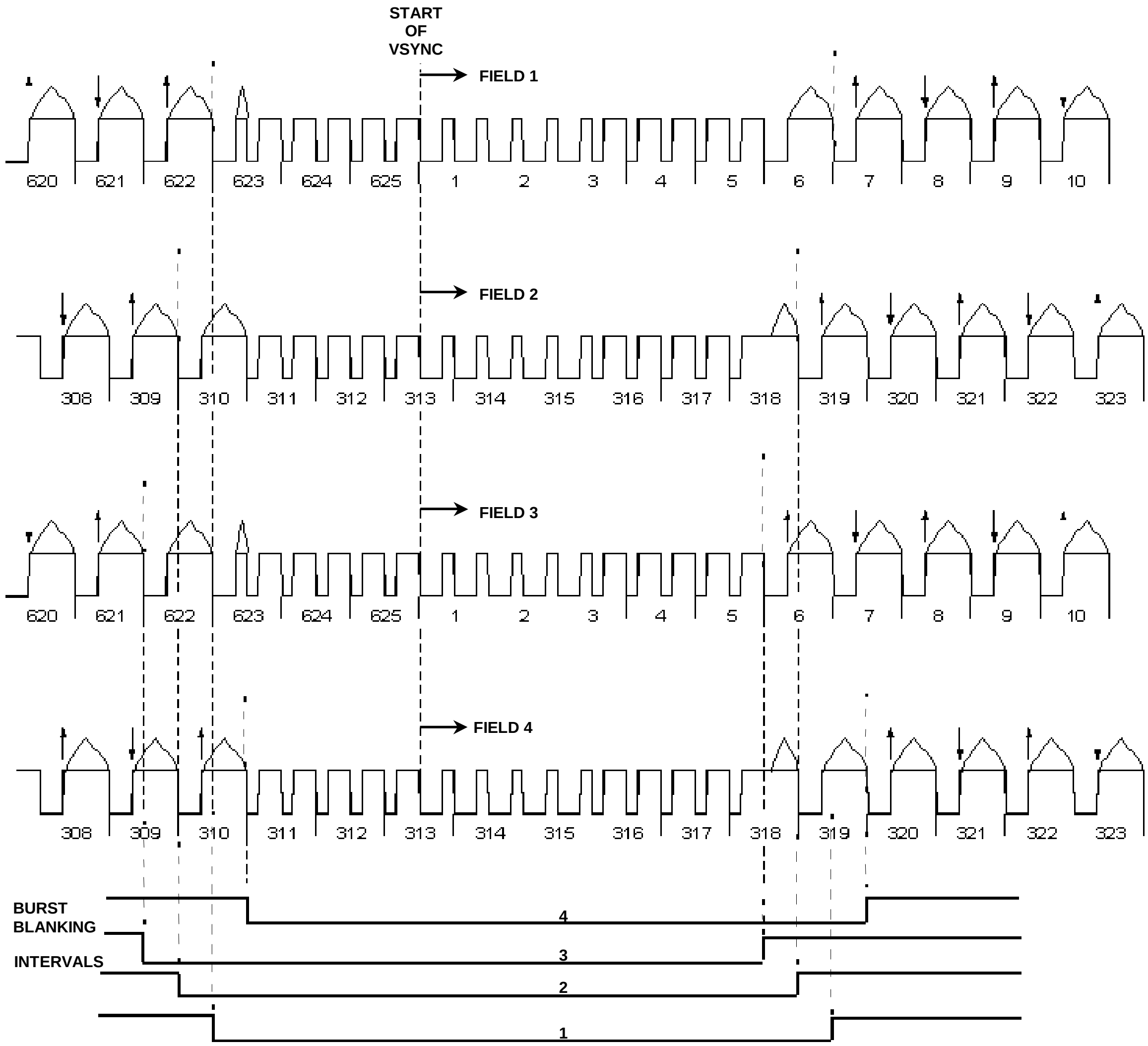

Figure 11: Interlaced PAL Video Timing

Color/Level	mA	V
White	26.66	1.000
Yellow	24.66	0.925
Cyan	21.37	0.801
Green	19.37	0.726
Magenta	16.22	0.608
Red	14.22	0.533
Blue	11.08	0.415
Black	9.08	0.340
Blank	7.65	0.287
Sync	0.00	0.000

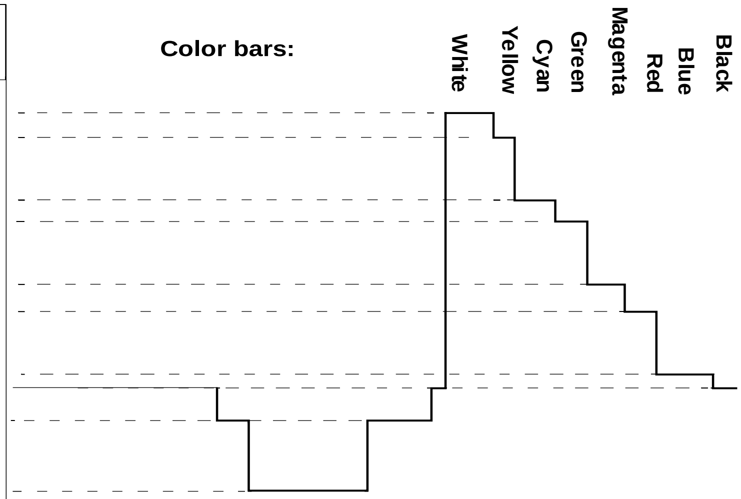

Figure 12: NTSC Y (Luminance) Output Waveform (DACG = 0)

Color/Level	mA	V
White	26.75	1.003
Yellow	24.62	0.923
Cyan	21.11	0.792
Green	18.98	0.712
Magenta	15.62	0.586
Red	13.49	0.506
Blue	10.14	0.380
Blank/ Black	8.00	0.300
Sync	0.00	0.000

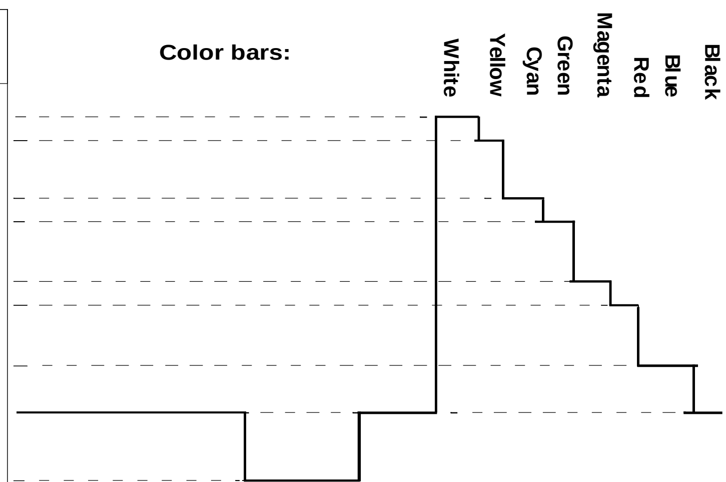

Figure 13: PAL Y (Luminance) Video Output Waveform (DACG = 1)

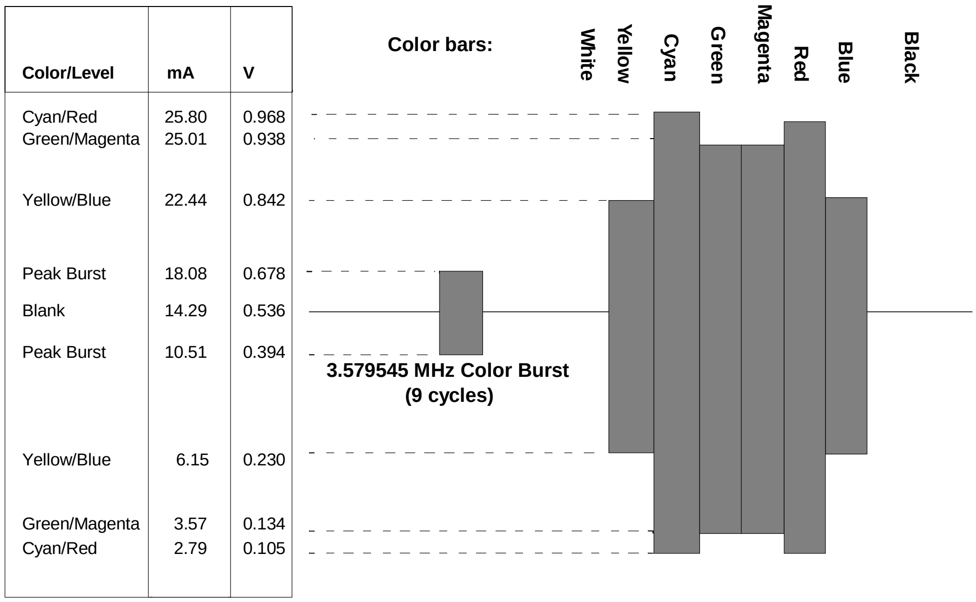

Figure 14: NTSC C (Chrominance) Video Output Waveform (DACG = 0)

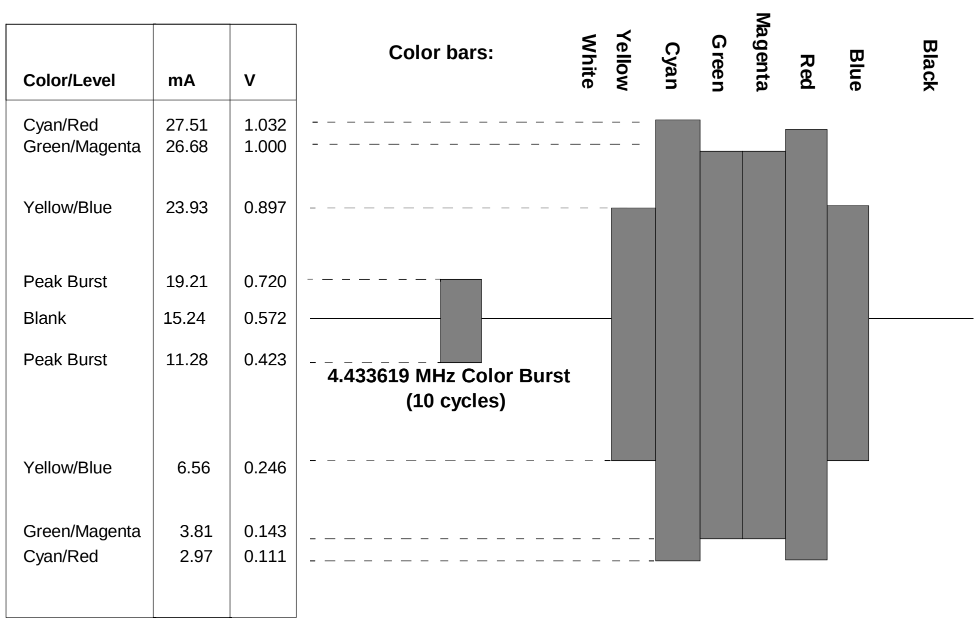

Figure 15: PAL C (Chrominance) Video Output Waveform (DACG = 1)

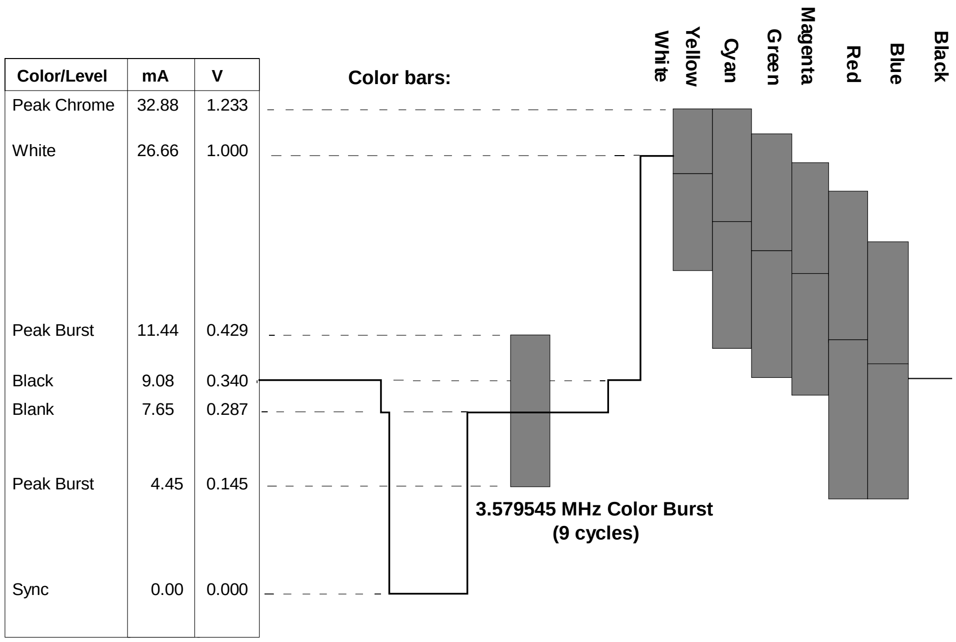

Figure 16: Composite NTSC Video Output Waveform (DACG = 0)

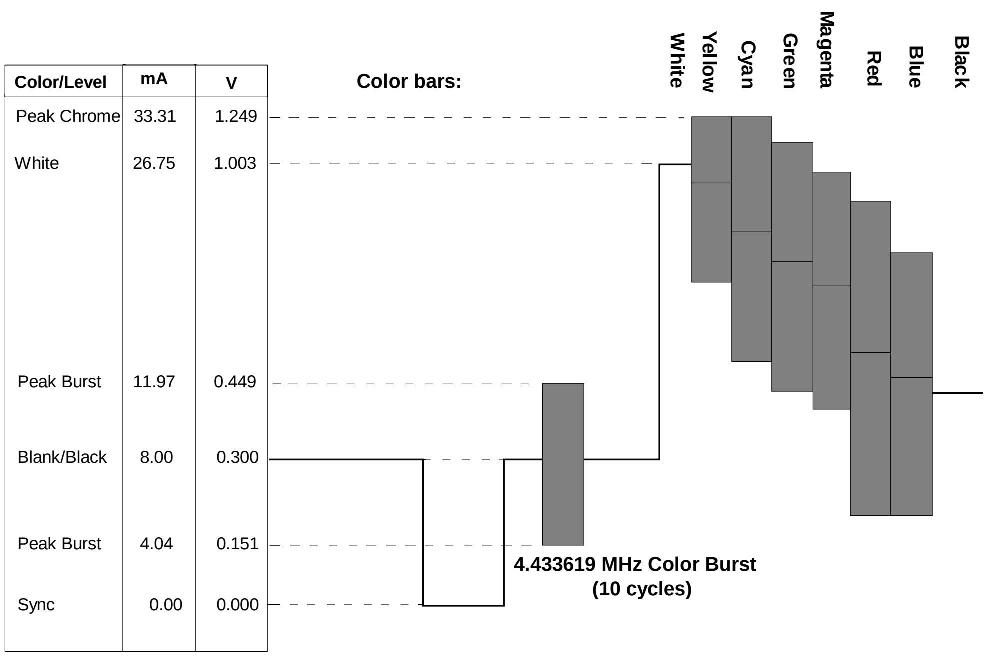

Figure 17: Composite PAL Video Output Waveform (DACG = 1)

3.3.5 TV Encoder / Bypass RGB / Component Video Outputs

The four TV encoder DAC outputs in the CH7019 can be switched to two sets of output pins DACA[3:0] and DACB[3:0] via video switches. This feature facilitates simple connection to two sets of video connectors as listed in Table 12 below:

Table 12: TV Output Configurations

	2 RCA + 1 S-Video	**SCART**
DACA0 (pin 47)	CVBS	B
DACA1 (pin 43)	Y	G
DACA2 (pin 45)	C	R
DACA3 (pin 41)	CVBS	CVBS
	VGA – Bypass RGB	**HDTV**
DACB0 (pin 46)	B	Pb
DACB1 (pin 42)	G	Y
DACB2 (pin 44)	R	Pr
DACB3 (pin 40)		CVBS

If the application calls for CVBS/S-video, SCART, RGB and YPrPb to output on the DAC output pins, different reconstruction filters for each type of signal can be implemented on the break-out cables.

The TV Encoder can be bypassed with input data driving the DACs directly. This mode can go to 165 MP/s. The CH7019 supports YPrPb output for driving 480i TV sets and SCART RGB for European TV.

3.4 LVDS-Out

Multiplexed input data, sync and clock signals from the graphics controllers input to the CH7019 through one of the two 12-bit variable voltage input ports, D1[11:0] or D2[11:0]. Non-multiplexed 24-bit input data input through both of the two input ports. For correct LVDS operation, the input data format must be selected to be IDFx=0, 1, 2, 3, 5, 8 or 9. Note for 24-bit formats, IDF1 must be set equal to IDF2.

If the two 12-bit input ports are driven from different timing generators then data can be sent to both the LVDS data path and the DACs in the TV data path. The DACs can output these data at 165 M pixels/sec to drive a second CRT monitor.

3.4.1 Single LVDS Channel Signal Mapping

Table 13: Signal Mapping for Single LVDS Channel

	18-bit
LDC[0](1)	R0
LDC[0](2)	R1
LDC[0](3)	R2
LDC[0](4)	R3
LDC[0](5)	R4
LDC[0](6)	R5
LDC[0](7)	G0
LDC[1](1)	G1
LDC[1](2)	G2
LDC[1](3)	G3
LDC[1](4)	G4
LDC[1](5)	G5
LDC[1](6)	B0
LDC[1](7)	B1
LDC[2](1)	B2
LDC[2](2)	B3
LDC[2](3)	B4
LDC[2](4)	B5
LDC[2](5)	HSYNC
LDC[2](6)	VSYNC
LDC[2](7)	DE

3.4.2 Dual LVDS Channel Signal Mapping

Table 14: Signal Mapping for Dual LVDS Channel

	18-bit
LDC[0](1)	Ro0
LDC[0](2)	Ro1
LDC[0](3)	Ro2
LDC[0](4)	Ro3
LDC[0](5)	Ro4
LDC[0](6)	Ro5
LDC[0](7)	Go0
LDC[1](1)	Go1
LDC[1](2)	Go2
LDC[1](3)	Go3
LDC[1](4)	Go4
LDC[1](5)	Go5
LDC[1](6)	Bo0
LDC[1](7)	Bo1
LDC[2](1)	Bo2
LDC[2](2)	Bo3
LDC[2](3)	Bo4
LDC[2](4)	Bo5
LDC[2](5)	HSYNC
LDC[2](6)	VSYNC
LDC[2](7)	DE
LDC[4](1)	Re0
LDC[4](2)	Re1
LDC[4](3)	Re2
LDC[4](4)	Re3
LDC[4](5)	Re4
LDC[4](6)	Re5
LDC[4](7)	Ge0
LDC[5](1)	Ge1
LDC[5](2)	Ge2
LDC[5](3)	Ge3
LDC[5](4)	Ge4
LDC[5](5)	Ge5
LDC[5](6)	Be0
LDC[5](7)	Be1
LDC[6](1)	Be2
LDC[6](2)	Be3
LDC[6](3)	Be4
LDC[6](4)	Be5
LDC[6](5)	LCTLE [1]
LDC[6](6)	LCTLF [1]
LDC[6](7)	LA6RL [1]

Note:
1. See description for register 65h.

3.4.3 Dithering

The dither engine in the CH7019 converts 24-bit per pixel to 18-bit per pixel RGB data before sending to the LVDS encoder. The 1D or the 2D dither algorithm can be selected via serial port programming. Maximum pixel rate supported is 165 M Pixels / sec. This function must be bypassed when pixel rate exceeds 165MHz.

3.4.4 Power Sequencing

The CH7019 conforms to SPWG's requirements on power sequencing. The timing specification shown in Figure 18 is a superset of the requirements dictated by the SPWG specification. The power sequencing block consists of a state machine and 5 hardware timers, which are programmable through serial port to suit requirements by different panels. It provides 2 signals ENAVDD and ENABKL to the LCD panel.

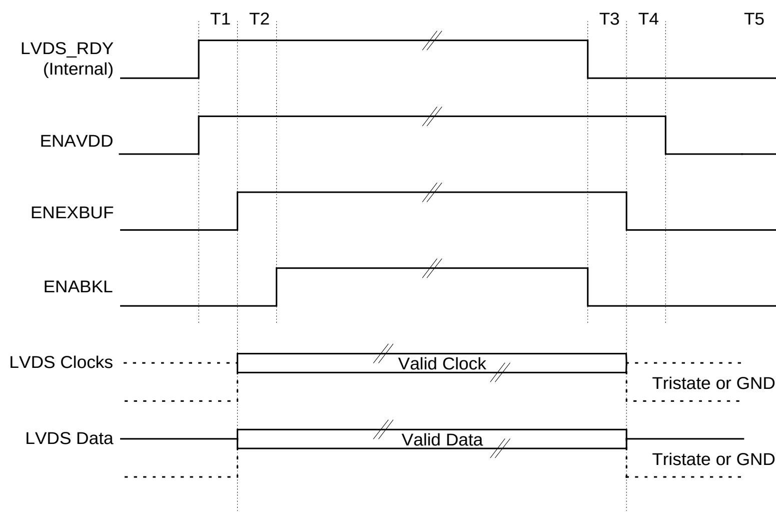

Figure 18: Power Sequencing

Table 15: Power Sequencing

	Range	Increment
T1	1-512 ms	1 ms
T2	2-256 ms	2ms
T3	2-256 ms	2ms
T4	1-512 ms	1 ms
T5	0-1600 ms	50ms

Power-on sequence begins when the LVDS software registers are set properly via serial port and the internal PLL lock detection circuit and the internal Sync detection circuits (see section 3.4.5) indicate that HSYNC, VSYNC and XCLK are stable. Note that the BKLEN bit (register 66h) must be set in order for the ENABKL signal to be asserted. Power-off sequence begins when any detection circuits indicate an instability in the timing signals (see section 3.4.5), or through software programming. Once power-off sequence starts, the internal state machine will complete the sequence and power-on sequence is allowed only after T5 is passed.

When the LVDS output clock and data signals become invalid, these outputs are tri-stated or grounded depending on the value of the LODP bit.

3.4.5 Panel Protection

The LCD panel can be damaged if HSYNC is absent from the LVDS link. This situation can happen when there is a catastrophic failure in the PC or the graphics system. The CH7019 is designed to prevent damage to the panel under such a failure. If the system fails, the CH7019 does not expect any software instruction from the graphics controller to power down the panel. Detection circuits are used to monitor the three timing signals – HSYNC, VSYNC and XCLK. If any one, combination of, or all of these signals becomes unstable, the CH7019 will commence Power Down Sequencing according to section 3.4.4. A description of these detection circuits is shown in Figure 19.

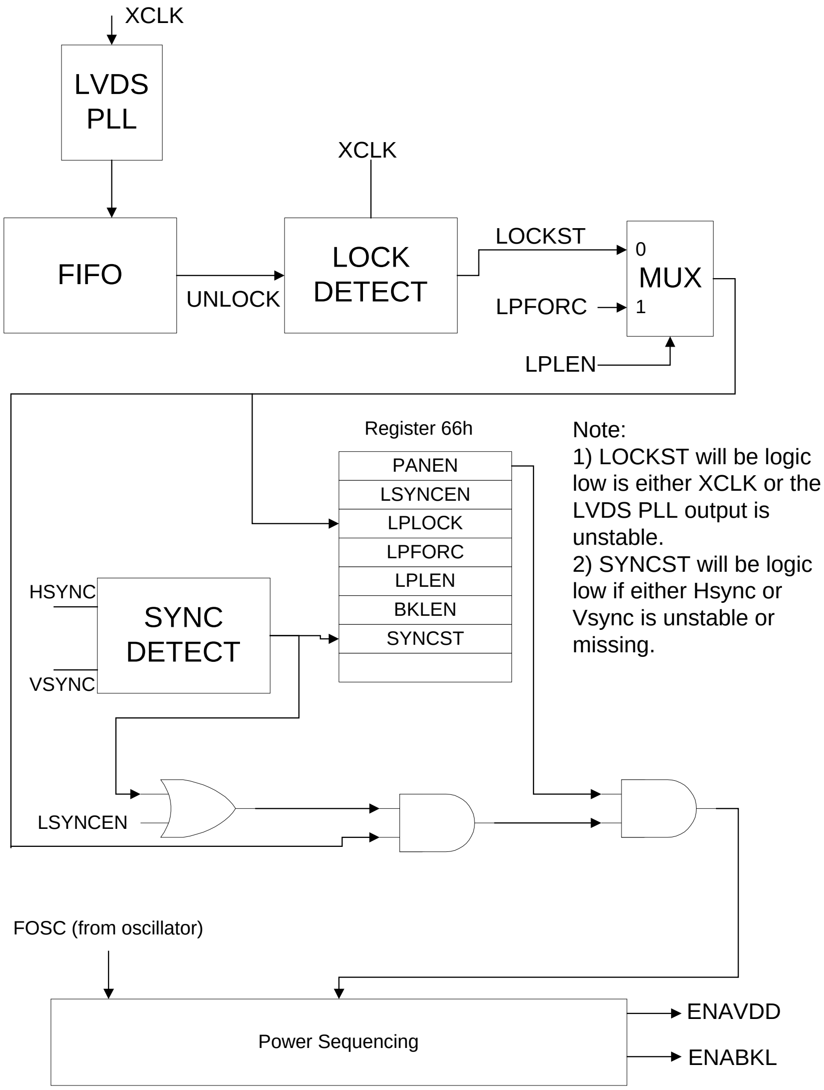

Figure 19: Detection Circuits for Panel Protection

The power up sequence can occur only if (a) XCLK is not missing, (b) there are no missing HSYNC and VSYNC, (c) the PLL CLOCK is stable, and (d) PANEN is set to 1. The power down sequence happens if any of those conditions fails. The power up sequence can also occur if the panel protection circuitry is bypassed.

The panel protection circuitry is comprised of a LOCKDET block, which detects an unstable clock from the LVDS PLL, a SYNCDET block, which detects missing inputs HSYNC and VSYNC, and an XCLK Detect block, which detects missing XCLK. XCLK stability (assuming it is not missing) is determined by the number of PLL unlock signals generated within one frame. This number is programmable via serial port using the BGLMT register (register 7Fh).

The SYNCDET block consists of counters to count HSYNC and VSYNC pulses. One counter is used to count the number of HSYNC pulses per frame over 3 frames. The end counts for all 3 frames must be equal to enable the power up sequence. In addition, the SYNCDET block checks for the presence of VSYNC and HSYNC. If VSYNC is missing for 2 frames or if HSYNC is missing for 32us the power up sequence is disabled. Conversely, if the panel has already been enabled and if the check of the number of HSYNC pulses over 3 frames yields different counts for any frame or if VSYNC is missing for 2 frames or if HSYNC is missing for 32us the CH7019 will go into a power down sequence.

The XCLK Detect block detects if XCLK is missing for more than approximately 1.2us.

The LOCKDET block and SYNCDET block can be defeated or bypassed independently through the LPMC register (register 66h) controls. To defeat the LOCKDET block set LPFORC to ‘1’ and LPLEN to ‘1’; to defeat the SYNCDET block set LSYNCEN to 1. The XCLK Detect block can be defeated or bypassed independently through the CLKDETD bit in register 14h, bit 2. To defeat the XCLK Detect block set CLKDETD to ‘1’.

The order of programming the control registers for the power up sequence is very important. **Both LPLOCK and SYNCST must read as 1 before setting PANEN to 1. Doing so will eliminate unexpected results on the LCD panel.**

3.4.6 EMI Spreading for Clock

LVDS data path can support a +- 2.5% spread spectrum clock to reduce EMI emission. The frequency and amplitude of the spread spectrum triangle waveform can be programmed via the serial port. Please refer to AN-59 for details.

3.5 Power Down

The CH7019 can be powered down under software control to achieve very low standby current. The matrix in table 16 shows the function of all the power down control bits for the CH7019. For a complete description of each individual bit please refer to the appropriate register description in sections 4.1 and 4.3.

Table 16: Power Down Control Bits

TVPD	DACPD3	DACPD2	DACPD1	DACPD0	LVDSPD	LODPDB1	LODPDB0	Description
1	X	X	X	X	1	X	X	Full Power Down
0	1	1	1	0	1	X	X	TV path powered up, DAC 0 on, DACs 1, 2, 3 off. LVDS path powered down.
0	0	0	0	1	1	X	X	TV path powered up, DAC 0 off, DACs 1, 2, 3 on. LVDS path powered down.
0	0	0	0	0	1	X	X	TV path powered up, DACs 0, 1, 2, 3 on. LVDS path powered down
1	X	X	X	X	0	0	0	TV path powered down LVDS path powered up. Both channels off..
1	X	X	X	X	0	0	1	TV path powered down. LVDS path powered up. Channel A on, channel B off.
1	X	X	X	X	0	1	0	TV path powered down. LVDS path powered up. Channel A off, channel B on.
1	X	X	X	X	0	1	1	TV path powered down. LVDS path powered up. Channel A on, channel B on.
0	0	0	0	0	0	1	1	TV path powered up, DACs 0, 1, 2, 3 on. LVDS path powered up. Channel A on, channel B on.

Note:
1. X = do not care.
2. TV bit (register 49h, bit 5) enables the TV path but does not control power down. In order for the TV path to function, TV must be set to 1 and TVPD set to 0.
3. An input channel which is routing data to an inactive path (TV or LVDS) is automatically powered down. For example, if PTSEL[1:0] = 10 (D1 input routed to TV and D2 input routed to LVDS) and if TVPD = 1 (TV path powered down) then data channel D1 is automatically powered down.
4. LDEN[1:0] (register 73h, bits 4-3) enable the LVDS outputs but do not control power down. In order for an LDVS channel to be active LVDSPD must be set to 0, the channel must be powered up (LODPDBx=1) and enabled (LDENx=1).