# Chrontel CH7301 DVI Output Device

## Features

- DVI Transmitter up to 165MHz
- DVI low jitter PLL
- DVI hot plug detection
- Provides 10-bit high speed video DAC for RGB output
- DAC connection detect
- Programmable power management
- Fully programmable through $I^2C$ port
- Complete Windows and DOS driver support
- Low voltage interface support to graphics device
- Offered in a 64-pin LQFP package

## General Description

The CH7301 is a Display controller device which accepts a digital graphics input signal, and encodes and transmits data through a DVI (TMDS™ link) or DFP (Digital flat panel) can also be supported. The device accepts data over one 12-bit wide variable voltage data port which supports four different RGB data formats.

The DVI processor includes a low jitter PLL for generation of the high frequency serialize clock, and all circuitry required to encode, serialize and transmit data. The CH7301 comes in versions able to drive a DFP display at a pixel rate of up to 165MHz, supporting UXGA resolution displays. No scaling of input data is performed on the data output to the DVI device.

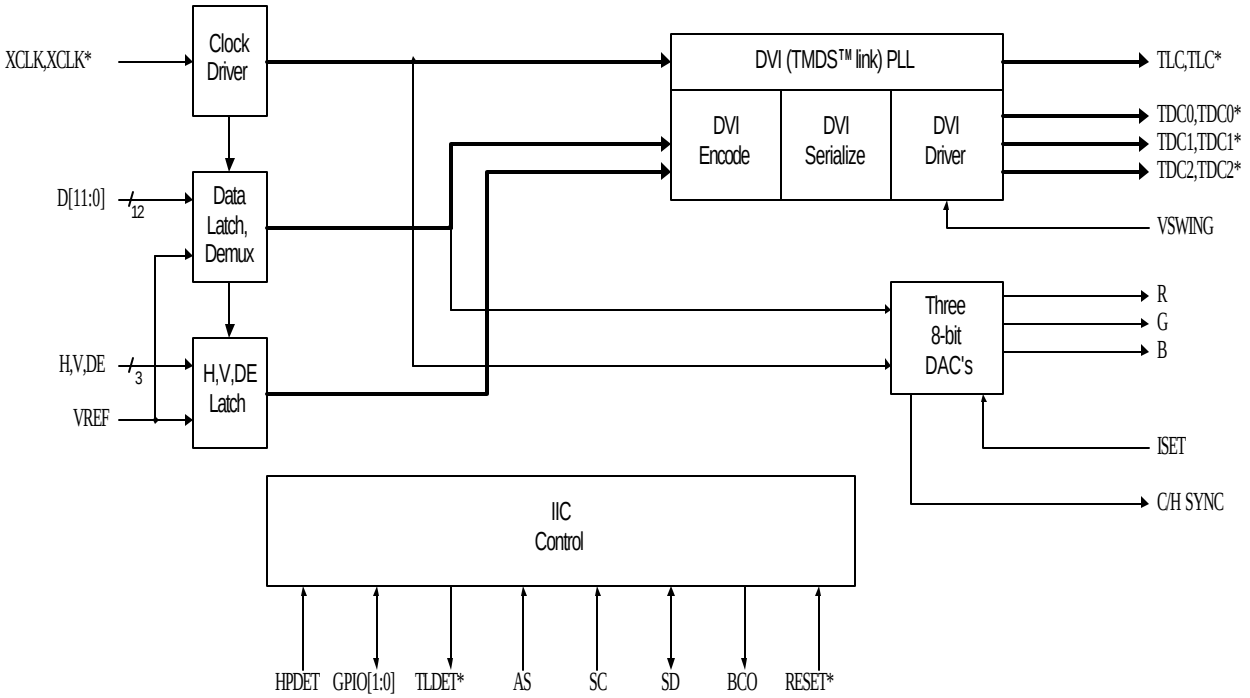



**Figure 1: Functional Block Diagram**

## Pin Descriptions

## Package Diagram

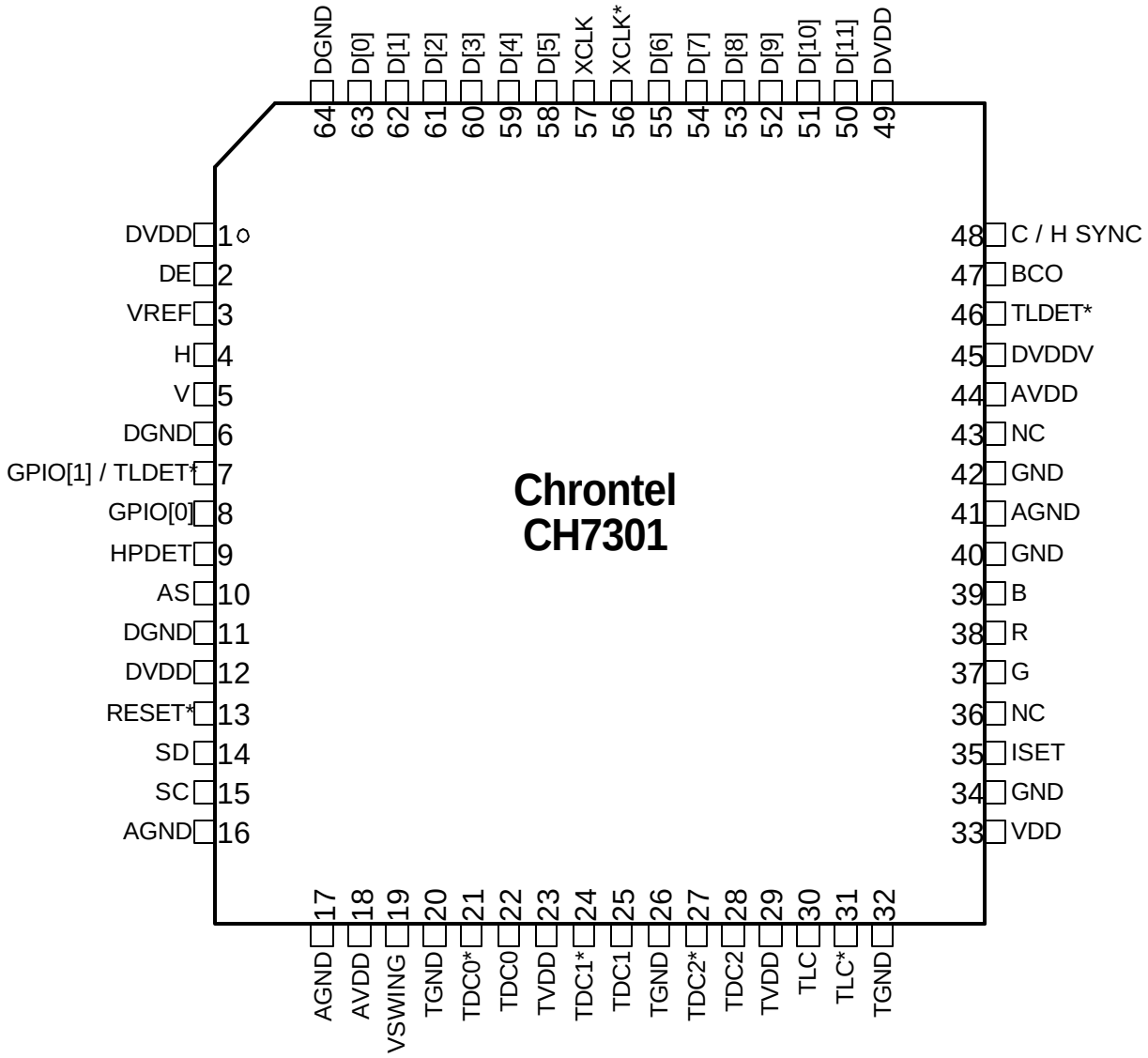



**Figure 2: 64-Pin LQFP**

**Table 1: Pin Description**

| 64-Pin LQFP | # Pins | Type | Symbol | Description |
|---|---|---|---|---|
| 2 | 1 | In | DE | **Data Enable**<br>This pin accepts a data enable signal which is high when active video data is input to the device, and low all other times. The levels are 0 to DVDDV, and the VREF signal is used as the threshold level. This input is used by the DVI links. |
| 3 | 1 | In | VREF | **Reference Voltage Input**<br>The VREF pin inputs a reference voltage of DVDDV / 2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, sync, data enable and clock inputs. |
| 4 | 1 | In/Out | H | **Horizontal Sync Input / Output**<br>This output is only for use with the TV-Out function. |
| 5 | 1 | In/Out | V | **Vertical Sync Input / Output**<br>This output is only for use with the TV-Out function. |
| 7 | 2 | In/Out | GPIO[1] /<br>TLDET* | **General Purpose Input - Output[1] /**<br>**DVI Link Detect Output** (internal pull-up)<br>This pin provides a general purpose I/O controlled via the IIC bus. The internal pull-up will be to the DVDD supply.<br>When the GPIO[1] pin is configured as an input, this pin can be used to output the DVI link detect signal (pulls low when a termination change has been detected on the HPDET input). This is an open drain output. The output is released through IIC control. |
| 8 | 2 | In/Out | GPIO[0] | **General Purpose Input - Output[0]** (internal pull-up)<br>This pin provides a general purpose I/O controlled via the IIC bus. The internal pull-up will be to the DVDD supply. |
| 9 | 1 | In | HPDET | **Hot Plug Detect** (internal pull-down)<br>This input pin determines whether the TMDS™ link is connected to a DVI monitor. When terminated, the monitor is required to apply a voltage greater than 2.4 volts. Changes on the status of this pin will be relayed to the graphics controller via the P-Out/TLDET* or GPIO[1]/TLDET* pin pulling low. |
| 10 | 1 | In | AS | **Address Select** (Internal pull-up)<br>This pin determines the IIC address of the device (1,1,1,0,1,AS*,AS). |
| 13 | 1 | In | RESET* | **Reset * Input** (Internal pull-up)<br>When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the IIC register. |
| 14 | 1 | In/Out | SD | **Serial Data Input / Output**<br>This pin functions as the serial data pin of the IIC interface port, and uses the DVDD supply. |
| 15 | 1 | In | SC | **Serial Clock Input**<br>This pin functions as the clock pin of the IIC interface port, and uses the DVDD supply. |
| 19 | 1 | In | VSWING | **DVI Link Swing Control**<br>This pin sets the swing level of the DVI outputs. A 2.4K ohm resistor should be connected between this pin and TGND using short and wide traces. |

**Table 1: Pin Description**

| 64-Pin LQFP | # Pins | Type | Symbol | Description |
|---|---|---|---|---|
| 22, 21 | 2 | Out | TDC0,<br>TDC0* | **TMDS™ Data Channel 0 Outputs**<br>These pins provide the TMDS™ differential outputs for data channel 0 (blue). |
| 25, 24 | 2 | Out | TDC1,<br>TDC1* | **TMDS™ Data Channel 1 Outputs**<br>These pins provide the TMDS™ differential outputs for data channel 1 (green). |
| 28, 27 | 2 | Out | TDC2,<br>TDC2* | **TMDS™ Data Channel 2 Outputs**<br>These pins provide the TMDS™ differential outputs for data channel 2 (red). |
| 30, 31 | 2 | Out | TLC,<br>TLC* | **TMDS™ Link Clock Outputs**<br>These pins provide the differential clock output for the TMDS™ interface corresponding to data on the TDC[0:2] outputs. |
| 35 | 1 | In | ISET | **Current Set Resistor Input**<br>This pin sets the DAC current. A 140 ohm resistor should be connected between this pin and GND (DAC ground) using short and wide traces. |
| 37 | 1 | Out | G | **Green Output** |
| 38 | 1 | Out | R | **Red Output** |
| 39 | 1 | Out | B | **Blue Output** |
| 43 | 1 | | NC | **No Connect** |
| 46 | 1 | Out | TLDET* | **DVI Link Detect Output**<br>This pin provides an open drain output which pulls low when a termination change has been detected on the HPDET input. The output is released through IIC control. |
| 47 | 1 | Out | BCO | **Buffered Clock Output**<br>This output pin provides a buffered clock output, driven by the DVDD supply. The output clock can be selected using the BCO register. |
| 48 | 1 | Out | C/H SYNC | **Composite / Horizontal Sync Output**<br>This pin is only for use with the TV-Out function. |
| 50 – 55,<br>58 – 63 | 12 | In | D[11] - D[0] | **Data[11] through Data[0] Inputs**<br>These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to DVDDV, and the VREF signal is used as the threshold level. |
| 57, 56 | 2 | In | XCLK,<br>XCLK* | **External Clock Inputs**<br>These inputs form a differential clock signal input to the CH7301 for use with the H, V, DE and D[11:0] data. If differential clocks are not available, the XCLK* input should be connected to VREF.<br><br>The output clocks from this pad cell are able to have their polarities reversed under the control of the MCP bit. |
| 1, 12, 49 | 3 | Power | DVDD | **Digital Supply Voltage (3.3V)** |
| 6, 11, 64 | 3 | Power | DGND | **Digital Ground** |
| 45 | 1 | Power | DVDDV | **I/O Supply Voltage (3.3V - 1.1V)** |
| 23, 29 | 2 | Power | TVDD | **DVI Transmitter Supply Voltage (3.3V)** |
| 20, 26, 32 | 3 | Power | TGND | **DVI Transmitter Ground** |
| 18, 44 | 2 | Power | AVDD | **PLL Supply Voltage (3.3V)** |
| 16, 17, 41,42 | 4 | Power | AGND | **PLL Ground** |
| 33 | 1 | Power | VDD | **DAC Supply Voltage (3.3V)** |
| 34, 36, 40 | 3 | Power | GND | **DAC Ground** |

## Mode of Operation

The CH7301 is capable of being operated as a single DVI output link. Descriptions of the single DVI output link operating mode, with a block diagram of the data flow within the device is shown below.

## DVI Output

In DVI Output mode, multiplexed input data, sync and clock signals are input to the CH7301 from the graphics controllers digital output port. Data will be 2X multiplexed, and the clock inputs can be 1X or 2X times the pixel rate. Some examples of modes supported are shown in the table below, and a block diagram of the CH7301 is shown on the following page. For the table below, clock frequencies for given modes were taken from VESA DISPLAY MONITOR TIMING SPECIFICATIONS if they were detailed there, not VESA TIMING DEFINITION FOR FLAT PANEL MONITORS. The device is not dependent upon this set of timing specifications. Any values of pixels/line, lines/frame and clock rate are acceptable, as long as the pixel rate remains below 165MHz. For correct DVI operation, the input data format must be selected to be one of the RGB input formats.

### Table 2: DVI Output

| Graphics Resolution | Active Aspect Ratio | Pixel Aspect Ratio | Refresh Rate (Hz) | XCLK Frequency (MHz) | DVI Frequency (MHz) |
|---|---|---|---|---|---|
| 720x400 | 4:3 | 1.35:1.00 | <85 | <35.5 | <355 |
| 640x400 | 8:5 | 1:1 | <85 | <31.5 | <315 |
| 640x480 | 4:3 | 1:1 | <85 | <36 | <360 |
| 720x480[1] | 4:3 | 9:8 | 59.94 | 27 | 270 |
| 720x576[1] | 4:3 | 15:12 | 50 | 27 | 270 |
| 800x600 | 4:3 | 1:1 | <85 | <57 | <570 |
| 1024x768 | 4:3 | 1:1 | <85 | <95 | <950 |
| 1280x720 | 16:9 | 1:1 | <60 | <67 | <670 |
| 1280x1024 | 4:3 | 1:1 | <85 | <158 | <1580 |
| 1600x1200 | 4:3 | 1:1 | <60 | <165 | <1650 |
| 1920x1080 | 16:9 | 1:1 | <30[2] | <140 | <1400 |

[1] These DVD compatible modes are input in a non-interlaced RGB data format

[2] 30Hz in progressive scan modes, 60Hz in interlaced modes

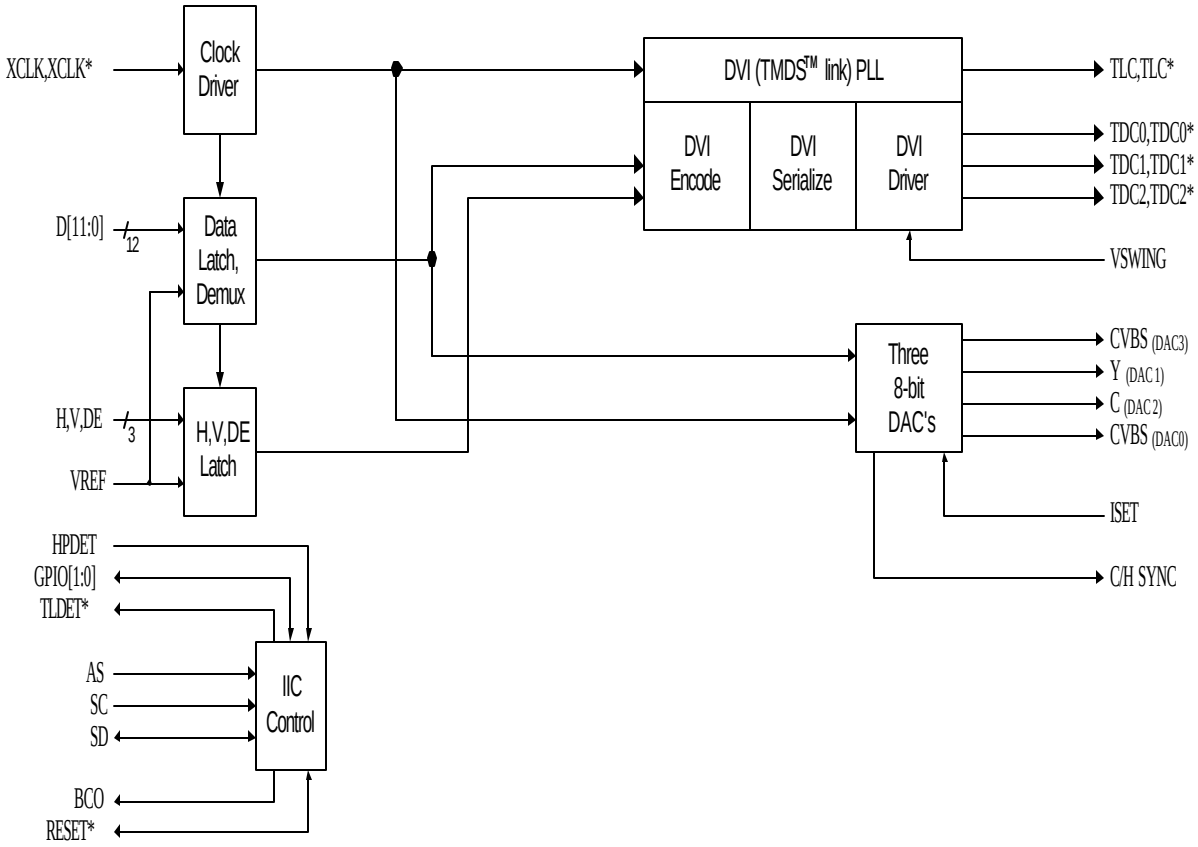



**Figure 3: DVI Output**

## Input Interface

Two distinct methods of transferring data to the CH7301 are described. They are:

- Multiplexed data, clock input at 1X pixel rate
- Multiplexed data, clock input at 2X pixel rate

For the multiplexed data, clock at 1X pixel rate the data applied to the CH7301 is latched with both edges of the clock (also referred to as dual-edge transfer mode). For the multiplexed data, clock at 2X pixel rate the data applied to the CH7301 is latched with one edge of the clock. The polarity of the pixel clock can be reversed under IIC control.

## Input Clock and Data Timing Diagram

The figure below shows the timing diagram for input data and clocks. The first XCLK/XCLK* waveform represents the input clock for the multiplexed data, clock at 2X pixel rate method. The second XCLK/XCLK* waveform represents the input clock for the multiplexed data, clock at 1X pixel rate method.

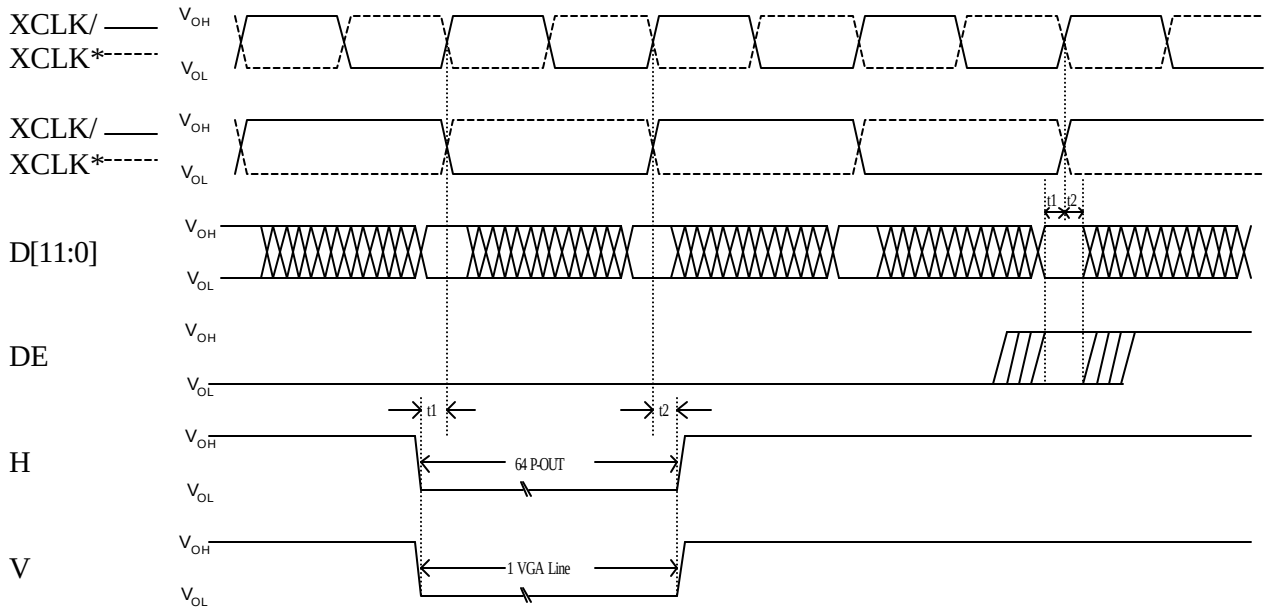



**Figure 4: Interface Timing**

**Table 3: Interface Timing**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{OH}$ | Output high level of interface signals | DVDDV - 0.2 | DVDDV + 0.2 | V |
| $V_{OL}$ | Output Low level of interface signals | -0.2 | 0.2 | V |
| t1[1] | D[11:0], H, V & DE to XCLK = XCLK* Delay (setup time) | TBD | | nS |
| t2[1] | XCLK = XCLK* to D[11:0], H, V & DE Delay (hold time) | TBD | | nS |
| DVDDV | Digital I/O Supply Voltage | 1.1 – 5% | 3.3 + 5% | V |

[1] D[11:0], H, V DE times measured when input equals Vref+100mV on rising edges, Vref-100mV on falling edges.

## Input Clock and Data Formats

The 12 data inputs support 5 different multiplexed data formats, each of which can be used with a 1X clock latching data on both clock edges, or a 2X clock latching data with a single edge. The data received by the CH7301 can be used to drive the DVI output or directly drive the DAC's. The multiplexed input data formats are (IDF[2:0]):

| IDF | Description |
|---|---|
| 0 | 12-bit multiplexed RGB input (24-bit color), (multiplex scheme 1) |
| 1 | 12-bit multiplexed RGB2 input (24-bit color), (multiplex scheme 2) |
| 2 | 8-bit multiplexed RGB input (16-bit color, 565) |
| 3 | 8-bit multiplexed RGB input (15-bit color, 555) |
| 4 | 8-bit multiplexed YCrCb input (24-bit color), (Y, Cr and Cb are multiplexed) |

For multiplexed input data formats, either both transitions of the XCLK/XCLK* clock pair, or each rising or falling edge of the clock pair (depending upon MCP bit, rising refers to a rising edge on the XCLK signal, a falling edge on the XCLK* signal) will latch data from the graphics chip. The multiplexed input data formats are shown in the figures below. The Pixel Data bus represents a 12-bit or 8-bit multiplexed data stream, which contains either RGB or YCrCb formatted data. The input data rate is 2X the pixel rate, and each pair of Pn values (eg; P0a and P0b) will contain a complete pixel encoded as shown in the tables below. It is assumed that the first clock cycle following the leading edge of the incoming horizontal sync signal contains the first word (Pxa) of a pixel, if an active pixel was present immediately following the horizontal sync. This does not mean that active data should immediately follow the horizontal sync, however. When the input is a YCrCb data stream the color-difference data will be transmitted at half the data rate of the luminance data, with the sequence being set as Cb, Y, Cr, Y, where Cb0,Y0,Cr0 refers to co-sited luminance and color-difference samples and the following Y1 byte refers to the next luminance sample, per CCIR-656 standards (the clock frequency is dependent upon the current mode, and is not 27MHz as specified in CCIR-656). All non-active pixels should be 0 in RGB formats, and 16 for Y and 128 for CrCb in YCrCb formats.

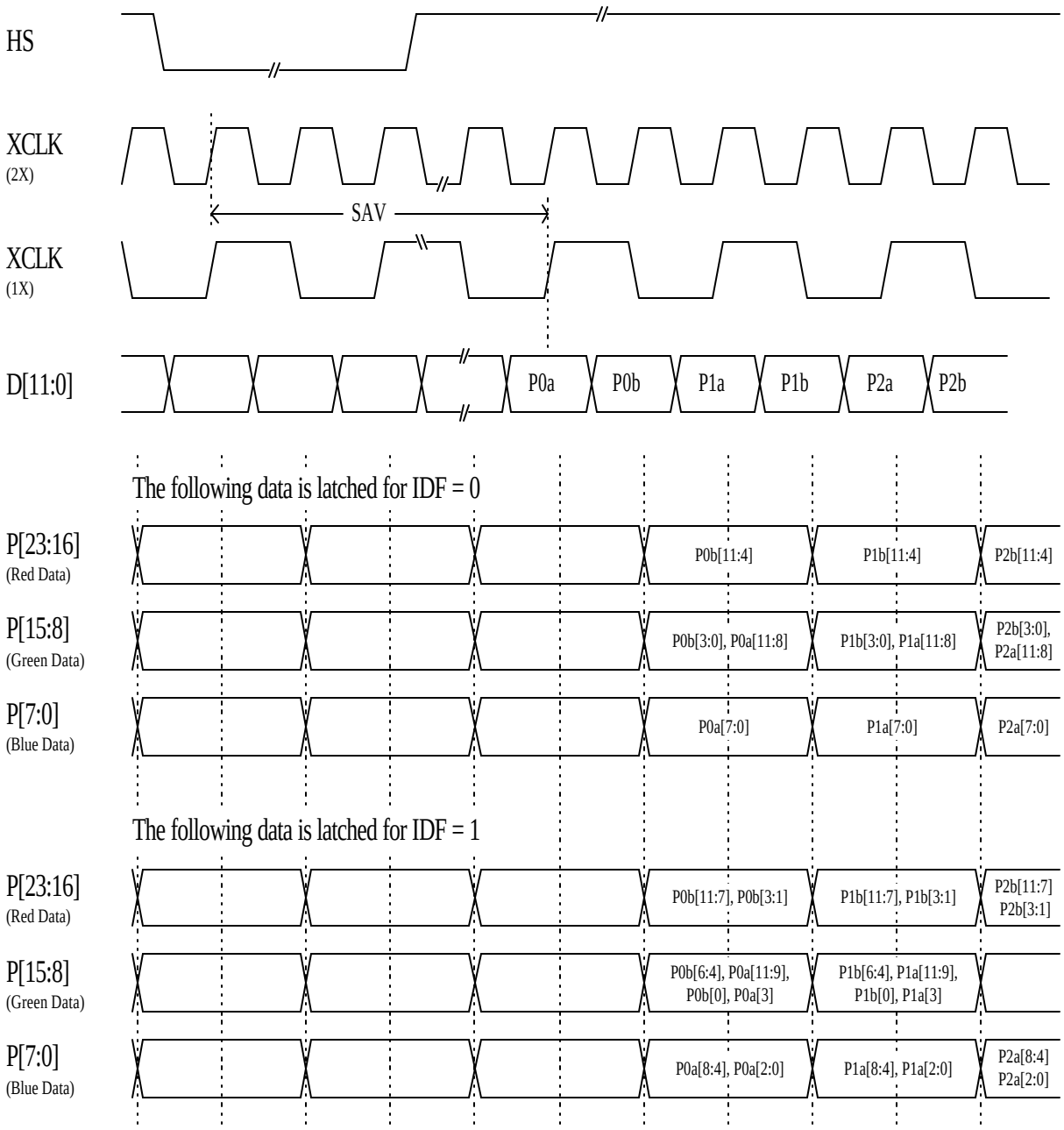



**Figure 5: Multiplexed Input Data Formats (IDF = 0, 1)**

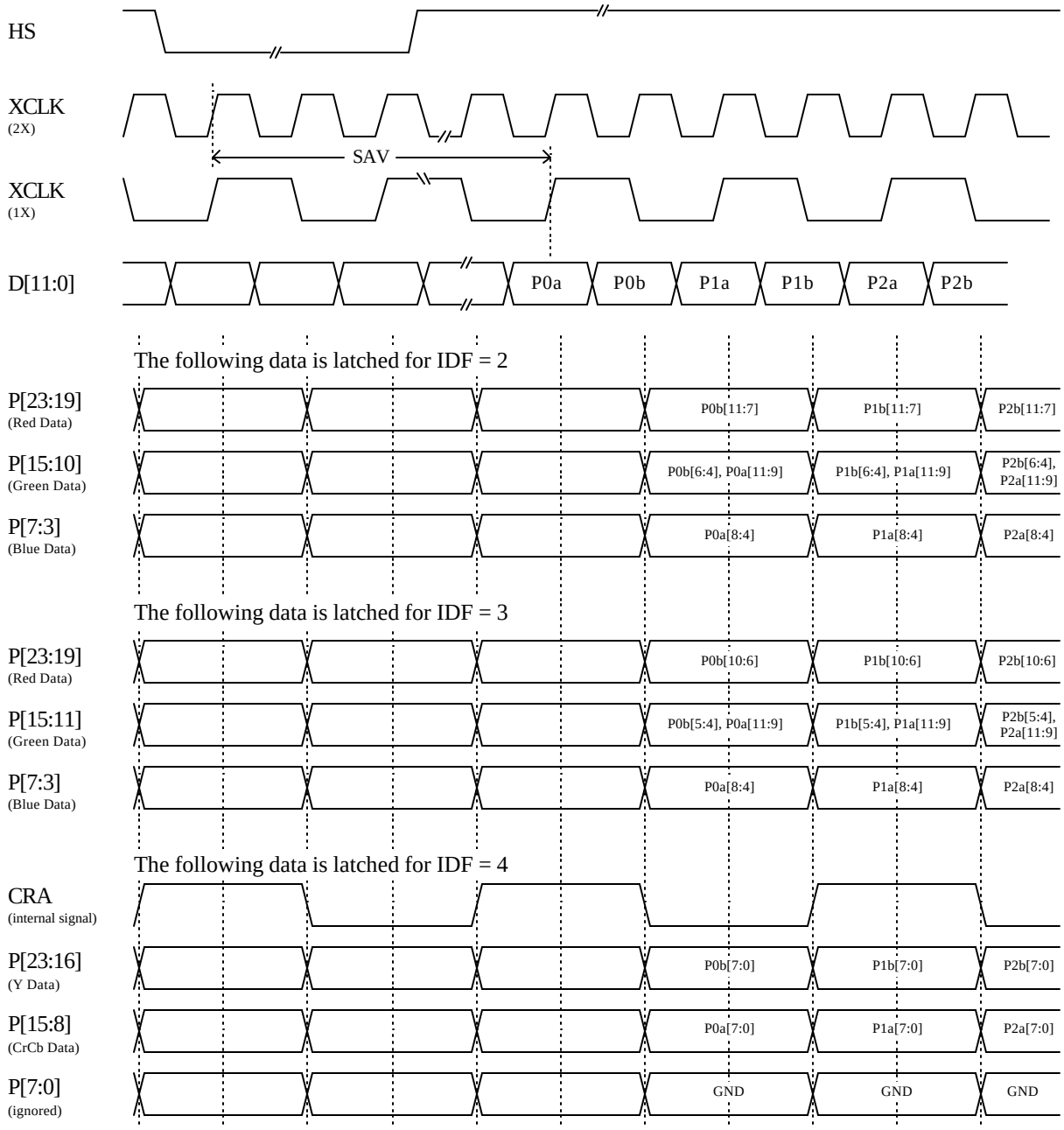



**Figure 6: Multiplexed Input Data Formats (IDF = 2, 3, 4)**

**Table 4: Multiplexed Input Data Formats (IDF = 0, 1)**

| IDF = | | 0 | | | | 1 | | | |
|---|---|---|---|---|---|---|---|---|---|
| Format = | | 12-bit RGB (12-12) | | | | 12-bit RGB (12-12) | | | |
| Pixel # | | P0a | P0b | P1a | P1b | P0a | P0b | P1a | P1b |
| Bus Data | D[11] | G0[3] | R0[7] | G1[3] | R1[7] | G0[4] | R0[7] | G1[4] | R1[7] |
| | D[10] | G0[2] | R0[6] | G1[2] | R1[6] | G0[3] | R0[6] | G1[3] | R1[6] |
| | D[9] | G0[1] | R0[5] | G1[1] | R1[5] | G0[2] | R0[5] | G1[2] | R1[5] |
| | D[8] | G0[0] | R0[4] | G1[0] | R1[4] | B0[7] | R0[4] | B1[7] | R1[4] |
| | D[7] | B0[7] | R0[3] | B1[7] | R1[3] | B0[6] | R0[3] | B1[6] | R1[3] |
| | D[6] | B0[6] | R0[2] | B1[6] | R1[2] | B0[5] | G0[7] | B1[5] | G1[7] |
| | D[5] | B0[5] | R0[1] | B1[5] | R1[1] | B0[4] | G0[6] | B1[4] | G1[6] |
| | D[4] | B0[4] | R0[0] | B1[4] | R1[0] | B0[3] | G0[5] | B1[3] | G1[5] |
| | D[3] | B0[3] | G0[7] | B1[3] | G1[7] | G0[0] | R0[2] | G1[0] | R1[2] |
| | D[2] | B0[2] | G0[6] | B1[2] | G1[6] | B0[2] | R0[1] | B1[2] | R1[1] |
| | D[1] | B0[1] | G0[5] | B1[1] | G1[5] | B0[1] | R0[0] | B1[1] | R1[0] |
| | D[0] | B0[0] | G0[4] | B1[0] | G1[4] | B0[0] | G0[1] | B1[0] | G1[1] |

**Table 5: Multiplexed Input Data Formats (IDF = 2, 3)**

| IDF = | | 2 | | | | 3 | | | |
|---|---|---|---|---|---|---|---|---|---|
| Format = | | RGB 5-6-5 | | | | RGB 5-5-5 | | | |
| Pixel # | | P0a | P0b | P1a | P1b | P0a | P0b | P1a | P1b |
| Bus Data | D[11] | G0[4] | R0[7] | G1[4] | R1[7] | G0[5] | X | G1[5] | X |
| | D[10] | G0[3] | R0[6] | G1[3] | R1[6] | G0[4] | R0[7] | G1[4] | R1[7] |
| | D[9] | G0[2] | R0[5] | G1[2] | R1[5] | G0[3] | R0[6] | G1[3] | R1[6] |
| | D[8] | B0[7] | R0[4] | B1[7] | R1[4] | B0[7] | R0[5] | B1[7] | R1[5] |
| | D[7] | B0[6] | R0[3] | B1[6] | R1[3] | B0[6] | R0[4] | B1[6] | R1[4] |
| | D[6] | B0[5] | G0[7] | B1[5] | G1[7] | B0[5] | R0[3] | B1[5] | R1[3] |
| | D[5] | B0[4] | G0[6] | B1[4] | G1[6] | B0[4] | G0[7] | B1[4] | G1[7] |
| | D[4] | B0[3] | G0[5] | B1[3] | G1[5] | B0[3] | G0[6] | B1[3] | G1[6] |

**Table 6: Multiplexed Input Data Formats (IDF = 4)**

| IDF = | | 4 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Format = | | YCrCb 8-bit | | | | | | | |
| Pixel # | | P0a | P0b | P1a | P1b | P2a | P2b | P3a | P3b |
| Bus Data | D[7] | Cb0[7] | Y0[7] | Cr0[7] | Y1[7] | Cb2[7] | Y2[7] | Cr2[7] | Y3[7] |
| | D[6] | Cb0[6] | Y0[6] | Cr0[6] | Y1[6] | Cb2[6] | Y2[6] | Cr2[6] | Y3[6] |
| | D[5] | Cb0[5] | Y0[5] | Cr0[5] | Y1[5] | Cb2[5] | Y2[5] | Cr2[5] | Y3[5] |
| | D[4] | Cb0[4] | Y0[4] | Cr0[4] | Y1[4] | Cb2[4] | Y2[4] | Cr2[4] | Y3[4] |
| | D[3] | Cb0[3] | Y0[3] | Cr0[3] | Y1[3] | Cb2[3] | Y2[3] | Cr2[3] | Y3[3] |
| | D[2] | Cb0[2] | Y0[2] | Cr0[2] | Y1[2] | Cb2[2] | Y2[2] | Cr2[2] | Y3[2] |
| | D[1] | Cb0[1] | Y0[1] | Cr0[1] | Y1[1] | Cb2[1] | Y2[1] | Cr2[1] | Y3[1] |
| | D[0] | Cb0[0] | Y0[0] | Cr0[0] | Y1[0] | Cb2[0] | Y2[0] | Cr2[0] | Y3[0] |

When IDF = 4 (YCrCb mode), the data inputs can also be used to transmit sync information to the device. In this mode, the embedded sync will follow the VIP2 convention, and the first byte of the 'video timing reference code' will be assumed to occur when a Cb sample would occur, if the video stream was continuous. This is shown below:

**Table 7: Embedded Sync**

| IDF = | | 4 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Format = | | YCrCb 8-bit | | | | | | | |
| Pixel # | | P0a | P0b | P1a | P1b | P2a | P2b | P3a | P3b |
| Bus Data | Dx[7] | FF | 00 | 00 | S[7] | Cb2[7] | Y2[7] | Cr2[7] | Y3[7] |
| | Dx[6] | FF | 00 | 00 | S[6] | Cb2[6] | Y2[6] | Cr2[6] | Y3[6] |
| | Dx[5] | FF | 00 | 00 | S[5] | Cb2[5] | Y2[5] | Cr2[5] | Y3[5] |
| | Dx[4] | FF | 00 | 00 | S[4] | Cb2[4] | Y2[4] | Cr2[4] | Y3[4] |
| | Dx[3] | FF | 00 | 00 | S[3] | Cb2[3] | Y2[3] | Cr2[3] | Y3[3] |
| | Dx[2] | FF | 00 | 00 | S[2] | Cb2[2] | Y2[2] | Cr2[2] | Y3[2] |
| | Dx[1] | FF | 00 | 00 | S[1] | Cb2[1] | Y2[1] | Cr2[1] | Y3[1] |
| | Dx[0] | FF | 00 | 00 | S[0] | Cb2[0] | Y2[0] | Cr2[0] | Y3[0] |

In this mode, the S[7..0] byte contains the following data:

S[6] = F = 1 during field 2, 0 during field 1

S[5] = V = 1 during field blanking, 0 elsewhere

S[4] = H = 1 during EAV (synchronization reference at the end of active video)

0 during SAV (synchronization reference at the start of active video)

Bits S[7] and S[3..0] are ignored

## Hot Plug Detection

The CH7301 has the capability of signaling to the graphics controller when the termination of the DVI outputs has changed. The operation of this circuit is as follows. The HPDET input pin of the CH7301 should be connected to pin 16 of the DVI connector. When a DVI monitor is connected to the DVI connector, this pin will be pulled high (above 2.4 volts). When a DVI monitor is not connected to the DVI connector, the internal pull-down on the HPDET pin will pull low. The CH7301 will detect any transition at the HPDET pin. When the HPIE (Hot Plug Interrupt Enable) bit in IIC register 1Eh is high, the CH7301 will pull low on the P-Out / TLDET* pin. When the HPIE2 (Hot Plug Interrupt Enable 2) bit in IIC register 20h is high, the CH7301 will pull low on the GPIO[1] / TLDET* pin. This should signal the driver to read the DVIT bit in register 20h to determine the state of the HPDET pin. The P-Out / TLDET* pin will continue to pull low until the driver sets the HPIR (Hot Plug Interrupt Reset) bit in register 1Eh high. The driver should then set the HPIR bit low.

## Register Control

The CH7301 is controlled via an IIC control port. The IIC bus uses only the SC clock to latch data into registers, and does not use any internally generated clocks so that the device can be written to in all power down modes. The device retains all register states

The CH7301 contains a total of 37 registers for user control.

## Control Registers Map

The controls are listed below, divided into three sections: general controls, input / output controls and DVI controls. A register map and register description follows.

### GENERAL CONTROLS

| | |
|---|---|
| ResetIB | Software IIC reset |
| ResetDB | Software datapath reset |
| PD[6:0] | Power down controls (DVIP, DVIL, , DACPD[2:0], Full, Partial) |
| VID[7:0] | Version ID register |
| DID[7:0] | Device ID register |
| TSTP[1:0] | Enable/select test pattern generation (color bar, ramp) |

### INPUT/OUTPUT CONTROLS

| | |
|---|---|
| XCM | XCLK 1X, 2X select |
| XCMD[7:0] | Delay adjust between XCLK and D[11:0] |
| MCP | XCLK polarity control |
| HPIE, HPIE2 | Hot plug detect interrupt enable |
| HPIR | Hot plug detect interrupt reset |
| IDF[2:0] | Input data format |
| IBS | Input buffer select |
| TERM[5:0] | Termination detect/check (DVI Link, DACT3, DACT2, DACT1, DACT0, SENSE) |
| BCOEN | Enable BCO Output |
| BCO[2:0] | Select output signal for BCO pin |
| BCOP | BCO polarity |
| GPIOL[1:0] | Read or write level for GPIO pins |
| GOENB[1:0] | Direction control for GPIO pins |
| SYNCO[1:0] | Enables/selects sync output for bypass modes |
| DACG[1:0] | DAC gain control |
| DACBP | DAC bypass |

### DVI CONTROLS

| | |
|---|---|
| TPPD[2:0] | DVI PLL phase detector trim |
| TPCP[1:0] | DVI PLL charge pump trim |
| TPVT[5:0] | DVI PLL VDD trim |
| TPVCO[10:0] | DVI PLL VCO trim |
| TPLPF[3:0] | DVI PLL low pass filter |
| DVID[3:0] | DVI transmitter drive strength |
| DVII | DVI output invert |
| CTL[3:0] | DVI control inputs |

## I²C Port Operation

The CH7301 contains a standard I²C control port, through which the control registers can be written and read. This port is comprised of a two-wire serial interface, pins SD (bidirectional) and SC, which can be connected directly to the SDB and SCB buses as shown in **Figure 7**.

The Serial Clock line (SC) is input only and is driven by the output buffer of the master device (also shown in **Figure 7**). The CH7301 acts as a slave, and generation of clock signals on the bus is always the responsibility of the master device. When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function. Data on the bus can be transferred up to 400 kbit/s.

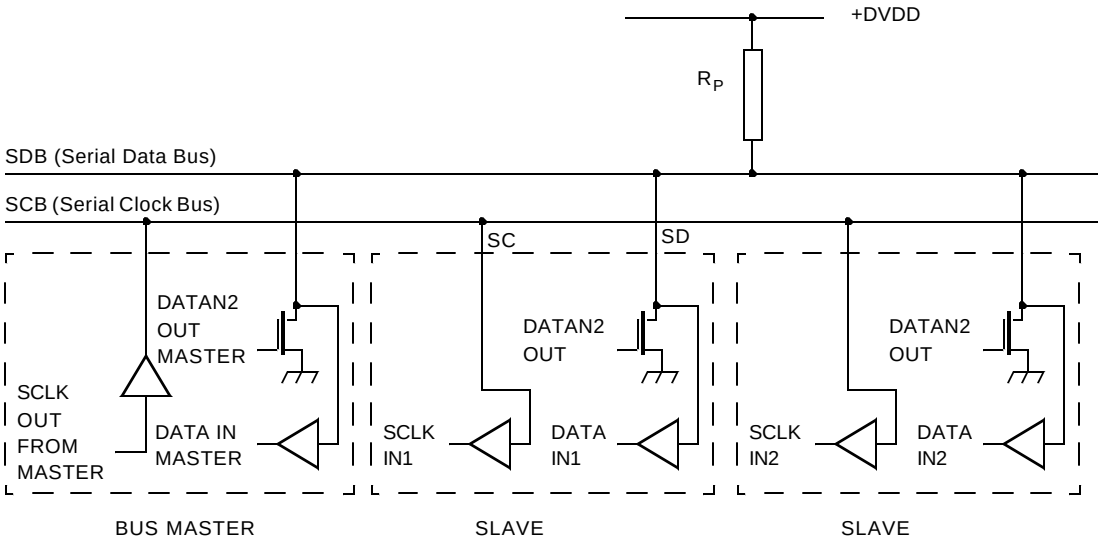



**Figure 7: Connection of Devices to the Bus**

### Electrical Characteristics for Bus Devices

The electrical specifications of the bus devices' inputs and outputs and the characteristics of the bus lines connected to them are shown in **Figure 7**. A pull-up resistor ($R_p$) must be connected to a 3.3V ± 10% supply. The CH7301 is a device with input levels related to DVDD.

#### Maximum and minimum values of pull-up resistor ($R_P$)

The value of $R_P$ depends on the following parameters:

- Supply voltage
- Bus capacitance
- Number of devices connected (input current + leakage current = $I_{input}$)

The supply voltage limits the minimum value of resistor $R_P$ due to the specified minimum sink current of 2mA at $VOL_{max}$ = 0.4 V for the output stages:

$$R_P >= (V_{DD} - 0.4) / 2 \quad (R_P \text{ in } k\Omega)$$

The bus capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of $R_P$ due to the specified rise time. The equation for RP is shown below:

$$R_P <= 10^3/C \quad \text{(where: } R_P \text{ is in } k\Omega \text{ and C, the total capacitance, is in pF)}$$

The maximum HIGH level input current of each input/output connection has a specified maximum value of 10 µA. Due to the desired noise margin of $0.2V_{DD}$ for the HIGH level, this input current limits the maximum value of $R_P$. The $R_P$ limit depends on $V_{DD}$ and is shown below:

$$R_P <= (100 \times V_{DD})/ I_{input} \quad \text{(where: } R_P \text{ is in } k\Omega \text{ and } I_{input} \text{ is in } \mu A)$$

## Transfer Protocol

Both read and write cycles can be executed in "Alternating" and "Auto-increment" modes. Alternating mode expects a register address prior to each read or write from that location (i.e., transfers alternate between address and data). Auto-increment mode allows you to establish the initial register location, then automatically increments the register address after each subsequent data access (i.e., transfers will be address, data...). A basic serial port transfer protocol is shown in **Figure 8** and described below.

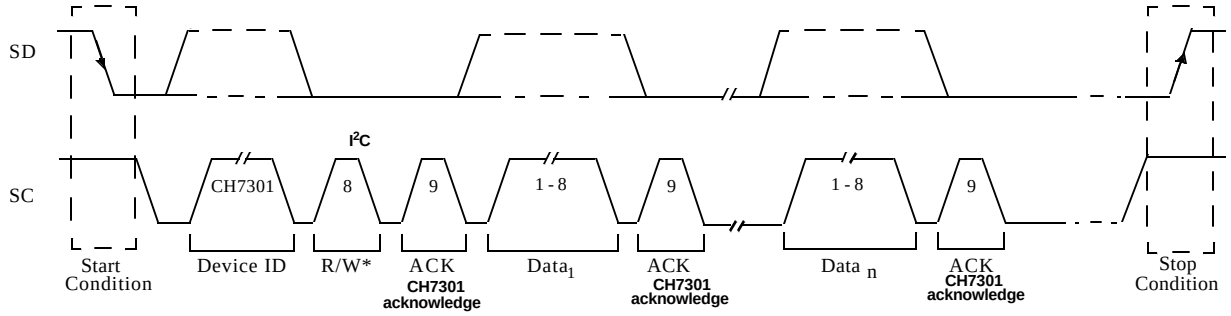



**Figure 8: Serial Port Transfer Protocol**

1. The transfer sequence is initiated when a high-to-low transition of SD occurs while SC is high; this is the "START" condition. Transitions of address and data bits can only occur while SC is low.
2. The transfer sequence is terminated when a low-to-high transition of SD occurs while SC is high; this is the "STOP" condition.
3. Upon receiving the first START condition, the CH7301 expects a Device Address Byte (DAB) from the master device. The value of the device address is shown in the DAB data format below.
4. After the DAB is received, the CH7301 expects a Register Address Byte (RAB) from the master. The format of the RAB is shown in the RAB data format below (note that B7 is not used).

### Device Address Byte (DAB)

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | R/W |

**R/W** **Read/Write Indicator**

"0": master device will write to the CH7301 at the register location specified by the address AR[6:0]

"1": master device will read from the CH7301 at the register location specified by the address AR[6:0].

### Register Address Byte (RAB)

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|
| 1 | AR[6] | AR[5] | AR[4] | AR[3] | AR[2] | AR[1] | AR[0] |

## Transfer Protocols *(continued)*

**AAR[6:0]** **Specifies the Address of the Register to be Accessed.**

This register address is loaded into the Address Register of the CH7301. The R/W access, which follows, is directed to the register specified by the content stored in the Address Register.

The following two sections describe the operation of the serial interface for the four combinations of R/W = 0,1 and AutoInc and alternating operation.

## CH7301 Write Cycle Protocols (R/W = 0)

Data transfer with acknowledge is required. The acknowledge-related clock pulse is generated by the master-transmitter. The master-transmitter releases the SD line (HIGH) during the acknowledge clock pulse. The slave-receiver must pull down the SD line, during the acknowledge clock pulse, so that it remains stable LOW during the HIGH period of the clock pulse. The CH7301 always acknowledges for writes (see **Figure 9**). Note that the resultant state on SD is the wired-AND of data outputs from the transmitter and receiver.

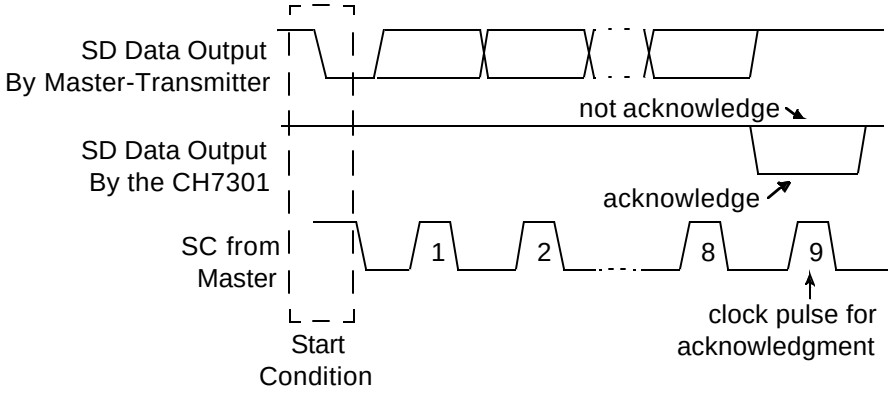
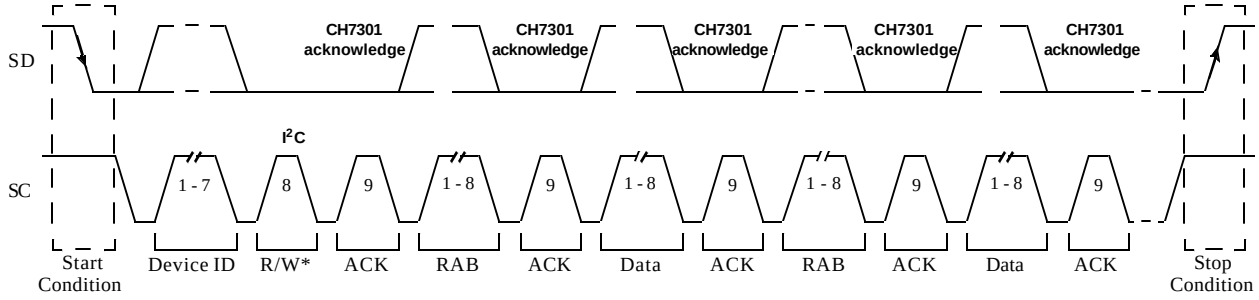



**Figure 9: Acknowledge on the Bus**

**Figure 10** shows two consecutive alternating write cycles. The byte of information, following the Register Address Byte (RAB), is the data to be written into the register specified by AR[6:0]. If AutoInc = 0, then another RAB is expected from the master device, followed by another data byte, and so on.

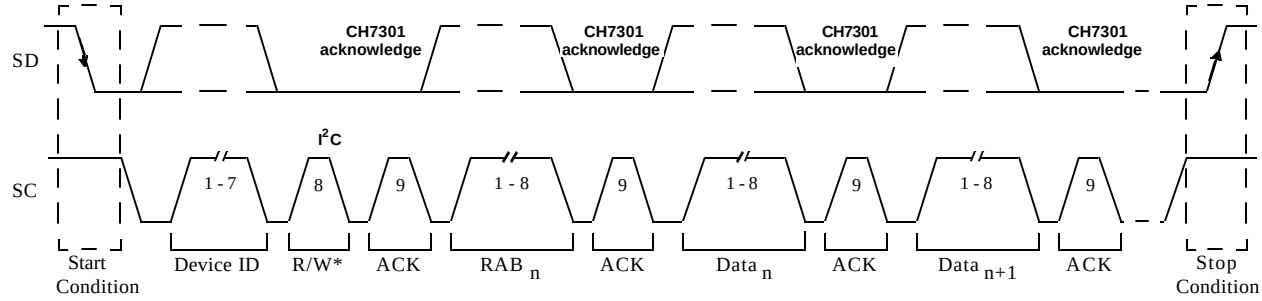



**Note:** The acknowledge is from the CH7301 (slave).

**Figure 10: Alternating Write Cycles**

If AutoInc = 1, then the register address pointer will be incremented automatically and subsequent data bytes will be written into successive registers without providing an RAB between each data byte. An Auto-increment write cycle is shown in **Figure 11**.

.




**Note:** The acknowledge is from the CH7301 (slave).

**Figure 11: Auto-Increment Write Cycle**

During auto-increment mode transfers, the register address pointer continues to increment for each write cycle until AR[6:0] = 4F. The next byte of information represents a new auto-sequencing "Starting address", which is the address of the register to receive the next byte. The auto-sequencing then resumes based on this new "Starting address". The auto-increment sequence can be terminated any time by either a "STOP" or "RESTART" condition. The write operation can be terminated with a "STOP" condition.

## CH7301 Read Cycle Protocols (R/W = 1)

If a master-receiver is involved in a transfer, it must signal the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter CH7301 releases the data line to allow the master to generate the STOP condition or the RESTART condition.

To read the content of the registers, the master device starts by issuing a "START" condition (or a "RESTART" condition). The first byte of data, after the START condition, is a DAB with R/W = 0. The second byte is the RAB with AR[6:0], containing the address of the register that the master device intends to read from in AR[6:0]. The master device should then issue a "RESTART" condition ("RESTART" = "START", without a previous "STOP" condition). The first byte of data, after this RESTART condition, is another DAB with R/W=1, indicating the master's intention to read data hereafter. The master then reads the next byte of data (the content of the register specified in the RAB). For alternating modes, another RESTART condition, followed by another DAB with R/W = 0 and RAB, is expected from the master device. The master device then issues another RESTART, followed by another DAB. After that, the master may read another data byte, and so on. In summary, a RESTART condition, followed by a DAB, must be produced by the master before each of the RAB, and before each of the data read events. Two consecutive alternating read cycles are shown in **Figure 12**.

## Transfer Protocols *(continued)*

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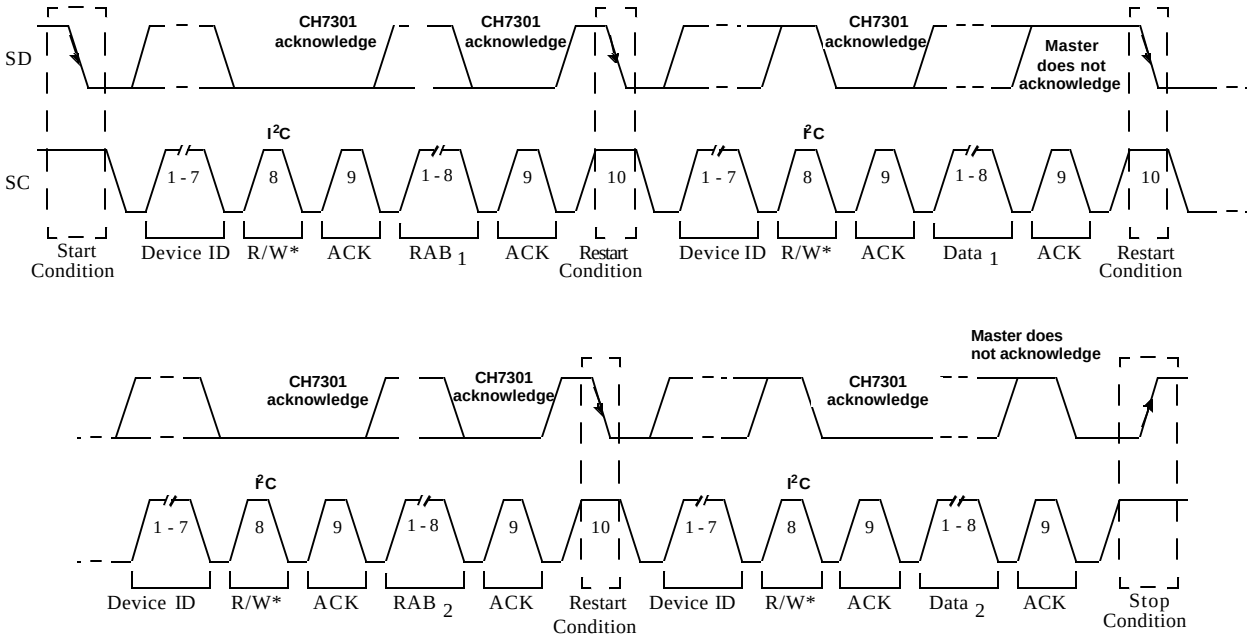



**Figure 12: Alternating Read Cycle**

For auto-increment reads the address register will be incremented automatically and subsequent data bytes can be read from successive registers, without providing a second RAB.

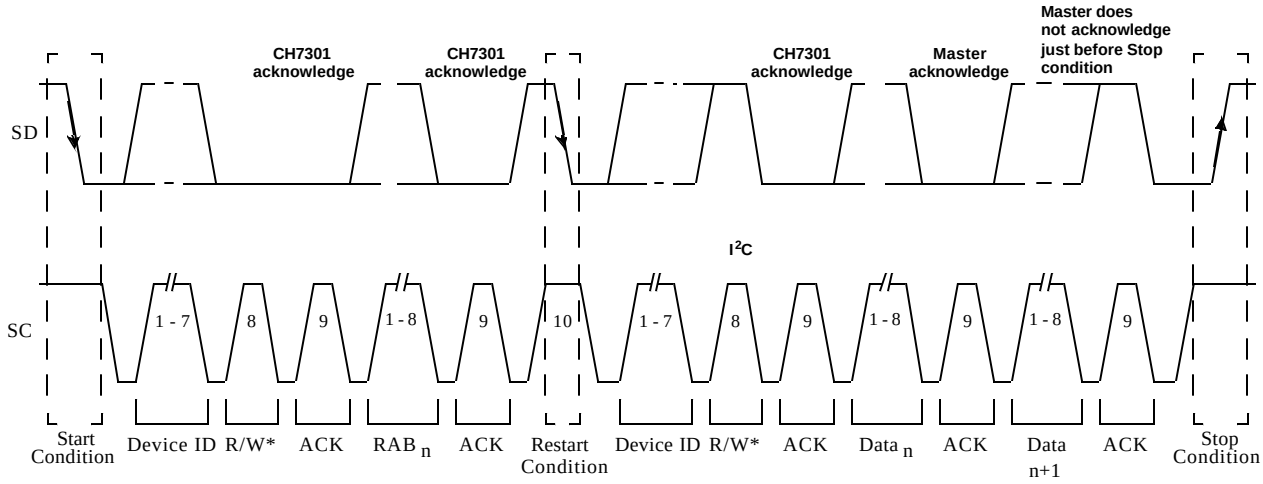



**Figure 13: Auto-increment Read Cycle**

When the auto-increment mode is enabled, the Address Register will continue incrementing for each read cycle. When the content of the Address Register reaches 4Fh, it will wrap around and start from 00h again. The auto increment sequence can be terminated by either a “STOP” or “RESTART” condition. The read operation can be terminated with a “STOP” condition. **Figure 13** shows an auto-increment read cycle terminated by a STOP or RESTART condition.

**Table 8: IIC Register Map w/o Macrovision**

| **Register** | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| 1Ch | | | | | Reserved | MCP | Reserved | XCM |
| 1Dh | | | | | XCMD3 | XCMD2 | XCMD1 | XCMD0 |
| 1Eh | GOENB1 | GOENB0 | GPIOL1 | GPIOL0 | HPIR | HPIE | Reserved | Reserved |
| 1Fh | IBS | Reserved | Reserved | Reserved | Reserved | IDF2 | IDF1 | IDF0 |
| 20h | HPIE2 | Reserved | DVIT | | DACT2 | DACT1 | DACT0 | SENSE |
| 21h | Reserved | Reserved | | SYNCO1 | SYNCO0 | DACG1 | DACG0 | DACBP |
| 22h | Reserved | Reserved | Reserved | BCOEN | BCOP | BCO2 | BCO1 | BCO0 |
| 31h | TPPD3 | TPPD2 | TPPD1 | TPPD0 | CTL3 | CTL2 | CTL1 | CTL0 |
| 32h | TPVCO7 | TPVCO6 | TPVCO5 | TPVCO4 | TPVCO3 | TPVCO2 | TPVCO1 | TPVCO0 |
| 33h | DVID2 | DVID1 | DVID0 | DVII | | | TPCP1 | TPCP0 |
| 35h | | | TPVT5 | TPVT4 | TPVT3 | TPVT2 | TPVT1 | TPVT0 |
| 36h | TPLPF3 | TPLPF2 | TPLPF1 | TPLPF0 | | | | |
| 37h | TPVCO10 | TPVCO9 | TPVCO8 | | | | | |
| 48h | | | | ResetIB | ResetDB | RSA | TSTP1 | TSTP0 |
| 49h | DVIP | DVIL | Reserved | DACPD3 | DACPD2 | DACPD1 | DACPD0 | FPD |
| 4Ah | VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 |
| 4Bh | DID7 | DID6 | DID5 | DID4 | DID3 | DID2 | DID1 | DID0 |

All register bits not defined in the register map are reserved bits, and should be left at the default value.

**Clock Mode Register**

**Symbol:** **CM**

**Address:** **1Ch**

**Bits:** **2**

| BIT: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SYMBOL: | | | | | Reserved | MCP | Reserved | XCM |
| TYPE: | | | | | R/W | R/W | R/W | R/W |
| DEFAULT: | | | | | 0 | 0 | 0 | 0 |

Bit 0 of register CM signifies the XCLK frequency. A value of '0' is used when the XCLK is at the pixel frequency (duel edge clocking mode) and a value of '1' is used when the XCLK is twice the pixel frequency (single edge clocking mode).

Bit 2 of register CM controls the phase of the XCLK clock input to the CH7301. A value of '1' inverts the XCLK signal at the input of the device. This control is used to select which edge of the XCLK signal to use for latching input data.

**Input Clock Register**

**Symbol:** **IC**

**Address:** **1Dh**

**Bits:** **8**

| BIT: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SYMBOL: | Reserved | Reserved | Reserved | Reserved | XCMD3 | XCMD2 | XCMD1 | XCMD0 |
| TYPE: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| DEFAULT: | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

Bits 3-0 of register IC controls the delay applied to the XCLK signal before latching input data.

**GPIO Control Register**

**Symbol:** **GPIO**

**Address:** **1Eh**

**Bits:** **8**

| BIT: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SYMBOL: | GOENB1 | GOENB0 | GPIOL1 | GPIOL0 | HPIR | HPIE | Reserved | Reserved |
| TYPE: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| DEFAULT: | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Bit 2 of register GPIO enables the hot plug interrupt detection signal to be output from the P-Out pin. A value of '1' allows the hot plug detect circuit to pull the TLDET* pin low when a change of state has taken place on the hot plug detect pin. A value of '0' disables the interrupt signal.

Bit 3 of register GPIO resets the hot plug detection circuitry. A value of '1' causes the CH7301 to release the TLDET* pin. When a hot plug interrupt is asserted by the CH7301, the CH7301 driver should read register 20h to determine the state of the DVI termination. After having read this register, the HPIR bit should be set high to reset the circuitry, and then set low again.

Bits 5-4 of register GPIO control the GPIO pins. When the corresponding GOENB bits are low, these register values are driven out of the corresponding GPIO pins. When the corresponding GOENB bits are high, these register values can be read to determine the level forced into the corresponding GPIO pins.

Bits 7-6 of register GPIO control the direction of the GPIO pins. A value of '1' sets the corresponding GPIO pin to an input, and a value of '0' sets the corresponding pin to an output.

**Input Data Format Register**

**Symbol:** **IDF**

**Address:** **1Fh**

**Bits:** **8**

| BIT: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SYMBOL: | IBS | | | | | IDF2 | IDF1 | IDF0 |
| TYPE: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| DEFAULT: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 2-0 of register IDF select the input data format. See Input Interface on page 5 for a listing of available formats.

Bit 7 of register IDF selects the input buffer used for the data, sync and clock input pins.

**Connection Detect Register**

**Symbol:** **CD**

**Address:** **20h**

**Bits:** **6**

| BIT: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SYMBOL: | HPIE2 | Reserved | DVIT | Reserved | DACT2 | DACT1 | DACT0 | SENSE |
| TYPE: | R/W | R/W | R | R | R | R | R | R/W |
| DEFAULT: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

The Connection Detect Register provides a means to determine the status of the DAC outputs and the DVI hot plug detect pin. The status bits, DACT[2:0] correspond to the termination of the three DAC outputs. However, the values contained in these STATUS BITS ARE NOT VALID until a sensing procedure is performed. Use of this register requires a sequence of events to enable the sensing of outputs, then reading out the applicable status bits. The detection sequence works as follows:

1) Set the power management register to enable all DAC's.

2) Set the SENSE bit to a 1. This forces a constant output from the DAC's. Note that during SENSE = 1, these 3 analog outputs are at steady state and no TV synchronization pulses are asserted.

3) Reset the SENSE bit to 0. This triggers a comparison between the voltage present on these analog outputs and the reference value. During this step, each of the four status bits corresponding to individual DAC outputs will be set if they are NOT CONNECTED.

4) Read the status bits. The status bits, DACT[2:0] now contain valid information which can be read to determine which outputs are connected to a TV. Again, a "0" indicates a valid connection, a "1" indicates an unconnected output.

Bit 5 of register CD can be read at any time to determine the level of the hot plug detect pin. When the hot plug detect pin changes state, and the DVI output is selected, the TLDET* output pin will be pulled low signifying a change in the DVI termination. At this point, the HPIR bit in register 1Eh should be set high, then low to reset the hot plug detect circuit.

Bit 7 of register CD enables the hot plug interrupt detection signal output from the GPIO[1] pin. A value of '1' allows the hot plug detect circuit to pull the GPIO[1] / TLDET* pin low when a change of state has taken place on the hot plug detect pin. A value of '0' disables the interrupt signal. The GOENB1 control bit in register 1Eh should be set to '1' when HPIE2 is set to '1'.

**DAC Control Register**

**Symbol:** **DC**

**Address:** **21h**

**Bits:** **6**

| BIT: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SYMBOL: | Reserved | Reserved | | SYNCO1 | SYNCO0 | DACG1 | DACG0 | DACBP |
| TYPE: | R/W | R/W | | R/W | R/W | R/W | R/W | R/W |
| DEFAULT: | 0 | 0 | | 0 | 0 | 0 | 0 | 0 |

Bit 0 of register DC selects the DAC bypass mode. A value of '1' outputs the incoming data directly at the DAC[2:0] outputs.

Bits 2-1 of register DC control the DAC gain. DACG0 should be set low for NTSC and PAL-M video standards, and high for PAL and NTSC-J video standards. DACG1 should be low when the input data format is RGB (IDF = 0-3), and high when the input data format is YCrCb (IDF = 4).

Bits 4-3 of register DC select the signal to be output from the C/H Sync pin according to **Table 9** below.

### Table 9: Composite / Horizontal Sync Output

| **SYNCO[1:0]** | C/H Sync Output |
|---|---|
| 00 | No Output |
| 01 | VGA Horizontal Sync |
| 10 | TV Composite Sync (Not Valid) |
| 11 | TV Horizontal Sync (Not Valid) |

**Buffered Clock Output Register**

**Symbol:** **BCO**

**Address:** **22h**

**Bits:** **8**

| BIT: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SYMBOL: | Reserved | Reserved | Reserved | BCOEN | BCOP | BCO2 | BCO1 | BCO0 |
| TYPE: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| DEFAULT: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 2-0 of register BCO select the signal output at the BCO pin, according to **Table 10** below:

### Table 10: BCO Output Signal

| **BCO[2:0]** | Buffered Clock Output | BCO[2:0] | Buffered Clock Output |
|---|---|---|---|
| 000 | (Not Valid) | 100 | (Not Valid) |
| 001 | (Not Valid) | 101 | (Not Valid) |
| 010 | (Not Valid) | 110 | VGA Vertical Sync |
| 011 | (Not Valid) | 111 | (Not Valid) |

Bit 3 of register BCO selects the polarity of the BCO output. A value of '1' does not invert the signal at the output pad.

Bit 4 of register BCO enables the BCO output. When BCOEN is high, the BCO pin will output the selected signal. When BCOEN is low, the BCO pin will be held in tri-state mode.

**DVI Control Input Register**

**Symbol:** **TCTL**

**Address:** **31h**

**Bits:** **8**

| BIT: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SYMBOL: | TPPD3 | TPPD 2 | TPPD 1 | TPPD 0 | CTL3 | CTL2 | CTL1 | CTL0 |
| TYPE: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| DEFAULT: | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 3-0 of register TCTL set the DVI control inputs applied to the green and red channels during sync intervals. It is recommended to leave these controls at the default value.

Bits 7-4 of register TCTL control the DVI PLL phase detector. The default value is recommended.

**DVI PLL VCO Control Register**

**Symbol:** **TVCO**

**Address:** **32h**

**Bits:** **8**

| BIT: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SYMBOL: | TPVCO7 | TPVCO6 | TPVCO5 | TPVCO4 | TPVCO3 | TPVCO2 | TPVCO1 | TPVCO0 |
| TYPE: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| DEFAULT: | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

Register TVCO controls the state of the DVI PLL VCO, and should be set according to the following tables.

**DVI PLL Charge Pump Control Register**

**Symbol:** **TPCP**

**Address:** **33h**

**Bits:** **5**

| BIT: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SYMBOL: | DVID2 | DVID1 | DVID0 | DVII | Reserved | Reserved | TPCP1 | TPCP0 |
| TYPE: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| DEFAULT: | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

Bits 1-0 of register TPCP control the DVI PLL charge pump. The default value is recommended.

Bits 3-2 of register TPCP are reserved bits, and should be left at the default value.

Bit 4 of register TPCP inverts the DVI outputs. A value of 1 inverts the outputs. A value of 0 is recommended.

Bits 7-5 of register TPCP control the DVI transmitter output drive level. The default value is recommended for DVI applications.

**DVI PLL Supply Control Register**

**Symbol:** **TPVT**
**Address:** **35h**
**Bits:** **5**

| BIT: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SYMBOL: | Reserved | Reserved | TPVT5 | TPVT4 | TPVT3 | TPVT2 | TPVT1 | TPVT0 |
| TYPE: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| DEFAULT: | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

Bits 5-0 of register TPVT control the DVI PLL supply voltage. The default value is recommended.

Bits 7-6 of register TPVT are reserved bits, and should be left at the default value.

**DVI PLL Filter Register**

**Symbol:** **TPF**
**Address:** **36h**
**Bits:** **8**

| BIT: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SYMBOL: | TPLPF3 | TPLPF2 | TPLPF1 | TPLPF0 | Reserved | Reserved | Reserved | Reserved |
| TYPE: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| DEFAULT: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Bits 3-0 of register TPT are reserved bits, and should be left at the default value.

Bits 7-4 of register TPT control the DVI PLL low pass filter. The default value is recommended.

**Test Pattern Register**

**Symbol:** **TSTP**
**Address:** **48h**
**Bits:** **5**

| BIT: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SYMBOL: | | | | ResetIB | ResetDB | RSA | TSTP1 | TSTP0 |
| TYPE: | | | | R/W | R/W | R/W | R/W | R/W |
| DEFAULT: | | | | 1 | 1 | 0 | 0 | 0 |

Bits 1-0 of register TSTP control the test pattern generation block. This test pattern can be used for both the DVI output and the TV Output. The pattern generated is determined by **Table 11** below.

### Table 11: Test Pattern Control

| **TSTP[1:0]** | Buffered Clock Output |
|---|---|
| 00 | No test pattern – Input data is used |
| 01 | Color Bars |
| 1 | Horizontal Luminance Ramp |

Bit 2 of register TSTP is a test control, and should be left at the default value.

Bit 3 of register TSTP controls the datapath reset signal. A value of '0' holds the datapath in a reset condition, while a value of '1', places the datapath in normal mode. The datapath is also reset at power on by an internally generated power on reset signal.

Bit 4 of register TSTP controls the IIC reset signal. A value of '0' holds the IIC registers in a reset condition, while a value of '1', places the IIC registers in normal mode. The IIC registers are also reset at power on by an internally generated power on reset signal.

**Power Management Register**

**Symbol:** **PM**

**Address:** **49h**

**Bits:** **8**

| BIT: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SYMBOL: | DVIP | DVIL | TV | Reserved | DACPD2 | DACPD1 | DACPD0 | FPD |
| TYPE: | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| DEFAULT: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Register TSTP controls which circuitry within the CH7301 is operating, according to **Table 12** below.

### Table 12: Power Management

| **Circuit Block** | Is Operational When |
|---|---|
| DVI PLL | DVIP = 1 & FPD != 1 |
| DVI Encode, Serialize and Transmitter | DVIL = 1 & FPD != 1 |
| VGA to TV Encoder | N/A |
| DAC 2 | DACPD2 != 1 & FPD != 1 |
| DAC 1 | DACPD1 != 1 & FPD != 1 |
| DAC 0 | DACPD0 != 1 & FPD != 1 |
| TV PLL, P-Out and BCO pins | FPD != 1 |

**Version ID Register**

**Symbol:** **VID**

**Address:** **4Ah**

**Bits:** **8**

| BIT: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SYMBOL: | VID7 | VID6 | VID5 | VID4 | VID3 | VID2 | VID1 | VID0 |
| TYPE: | R | R | R | R | R | R | R | R |
| DEFAULT: | MV | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Register VID is a read only register containing the version ID number of the CH7301. The MV default is '1' when the CH7301 is bonded out with Macrovision enabled, and '0' when the CH7301 is bonded out with Macrovision disabled.

**Device ID Register**

**Symbol:** **DID**

**Address:** **4Bh**

**Bits:** **8**

| BIT: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| SYMBOL: | DID7 | DID6 | DID5 | DID4 | DID3 | DID2 | DID1 | DID0 |
| TYPE: | R | R | R | R | R | R | R | R |
| DEFAULT: | TBD | TBD | TBD | TBD | TBD | TBD | TBD | TBD |

Register DID is a read only register containing the device ID number of the CH7301.

## Electrical Specifications

### Table 13. Absolute Maximum Ratings

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| | DVDD, AVDD, TVDD, VDD relative to GND | - 0.5 | | 5.0 | V |
| | Input voltage of all digital pins[1] | GND - 0.5 | | VDD + 0.5 | V |
| $T_{SC}$ | Analog output short circuit duration | | Indefinite | | Sec |
| $T_{AMB}$ | Ambient operating temperature | - 55 | | 85 | °C |
| $T_{STOR}$ | Storage temperature | - 65 | | 150 | °C |
| $T_J$ | Junction temperature | | | 150 | °C |
| $T_{VPS}$ | Vapor phase soldering (one minute) | | | 220 | °C |

**Notes:**

1. Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods my affect reliability.
2. The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce destructive latch.

### Table 14. Recommended Operating Conditions

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| VDD | DAC power supply voltage | 3.1 | 3.3 | 3.6 | V |
| AVDD | Analog supply voltage | 3.1 | 3.3 | 3.6 | V |
| DVDD | Digital supply voltage | 3.1 | 3.3 | 3.6 | V |
| TVDD, DVDDV | Digital supply voltage (P-OUT pin) | 1.1 | 1.8 | 3.6 | V |
| $R_L$ | Output load to DAC outputs | | 37.5 | | Ω |

### Table 15. Electrical Characteristics (Operating Conditions: $T_A = 0^oC - 70^oC$, $V_{DD} = 5V \pm 5\%$)

| | | | | | |
|---|---|---|---|---|---|
| | Video D/A resolution | 10 | 10 | 10 | Bits |
| | Full scale output current | | 33.89 | | mA |
| | Video level error | | | 10 | % |
| | VDD & AVDD current | | 90 | | mA |
| | DVDD, TVDD (3.3V) current | | TBD | | mA |
| | DVDD2 (1.8V) current (15pF load) | | 4 | | mA |

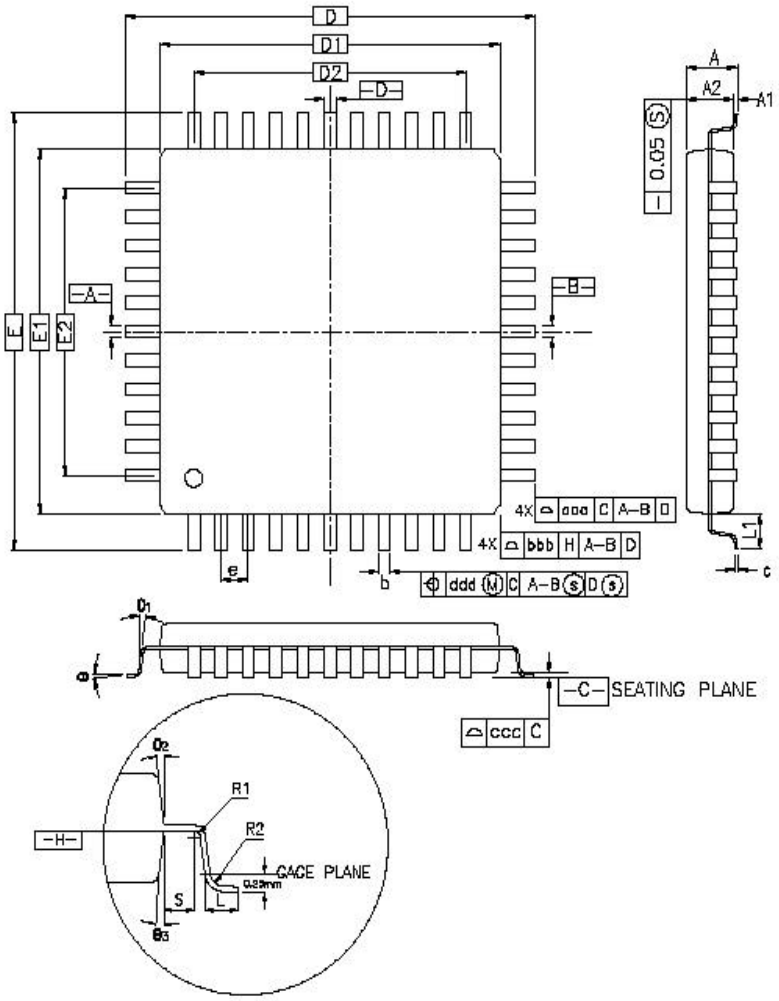
**Table 16. Digital Inputs / Outputs**

| Symbol | Description | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{SDOL}$ | SD Output Low Voltage | IOL = 2.0 mA | | | 0.4 | V |
| $V_{IICIH}$ | SD Input High Voltage | | 2.7 | | DVDD + 0.5 | V |
| $V_{IICIL}$ | SD Input Low Voltage | | GND-0.5 | | 1.4 | V |
| $V_{DATAIH}$ | D[0-11] Input High Voltage | | Vref-0.25 | | DVDD+0.5 | V |
| $V_{DATAIL}$ | D[0-11] Input Low Voltage | | GND-0.5 | | Vref+0.25 | V |
| $V_{P-OUTOH}$ | P-OUT Output High Voltage | IOL = - 400 µA | DVDDV-0.2 | | | V |
| $V_{P-OUTOL}$ | P-OUT Output Low Voltage | IOL = 3.2 mA | | | 0.2 | V |

**Note:**

$V_{IIC}$ -refers to $I^2C$ pins SD and SC.
$V_{DATA}$ - refers to all digital pixel and clock inputs.
$V_{SD}$ - refers to $I^2C$ pin SD as an output.
$V_{P-OUT}$ - refers to pixel data output Time - Graphics.

## Mechanical Package Information




CONTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.60 | — | — | 0.063 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 12.00 BSC. | | | 0.472 BSC. | | |
| D1 | 10.00 BSC. | | | 0.393 BSC. | | |
| E | 12.00 BSC. | | | 0.472 BSC. | | |
| E1 | 10.00 BSC. | | | 0.393 BSC. | | |
| R2 | 0.08 | — | 0.20 | 0.003 | — | 0.008 |
| R1 | 0.08 | — | — | 0.003 | — | — |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | — | — | 0° | — | — |
| θ2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | — | — | 0.008 | — | — |

| SYMBOL | 64L | | | | | |
|---|---|---|---|---|---|---|
| | MILLIMETER | | | INCH | | |
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| D2 | 7.50 | | | 0.295 | | |
| E2 | 7.50 | | | 0.295 | | |

TOLERANCES OF FORM AND POSITION

| | | |
|---|---|---|
| aaa | 0.20 | 0.008 |
| bbb | 0.20 | 0.008 |
| ccc | 0.08 | 0.003 |
| ddd | 0.08 | 0.003 |

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUN PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
   DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm FOR 0.4mm and 0.5mm PITCH PACKAGES.

| ORDERING INFORMATION | | | | |
|---|---|---|---|---|
| Part number | Package type | Number of pins | Voltage supply | Speed grade |
| CH7301A-T | LQFP | 64 | 3.3V | 115MHz |
| CH7301A-T-A | LQFP | 64 | 3.3V | 135MHZ |
| CH7301A-T-B | LQFP | 64 | 3.3V | 165MHZ |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