Chrontel CH7304 Single LVDS Transmitter

Features

- Single LVDS transmitter
- Supports pixel rate up to 165M pixels/sec
- Supports up to UXGA resolution (1600 x 1200)
- LVDS low jitter PLL
- LVDS 24-bit or 18-bit output
- 2D dither engine for 18-bit output
- Panel protection and power down sequencing
- Programmable power management
- Fully programmable through serial port
- Complete Windows and DOS driver support
- Variable voltage interface to graphics device
- Offered in a 64-pin LQFP package

1.0 General Description

The CH7304 is a Display Controller device, which accepts a graphics data stream over one 12-bit wide variable voltage (1.1V to 3.3V) port. The data stream outputs through an LVDS transmitter to an LCD panel. A maximum of 165M pixels per second can be output through a single LVDS link.

The LVDS transmitter supports 24-bit panels; it also includes a programmable dither function for support of 18-bit panels. Data is encoded into commonly used formats, including those detailed in the OpenLDI and the SPWG specification. Serialized data output on four differential channels.

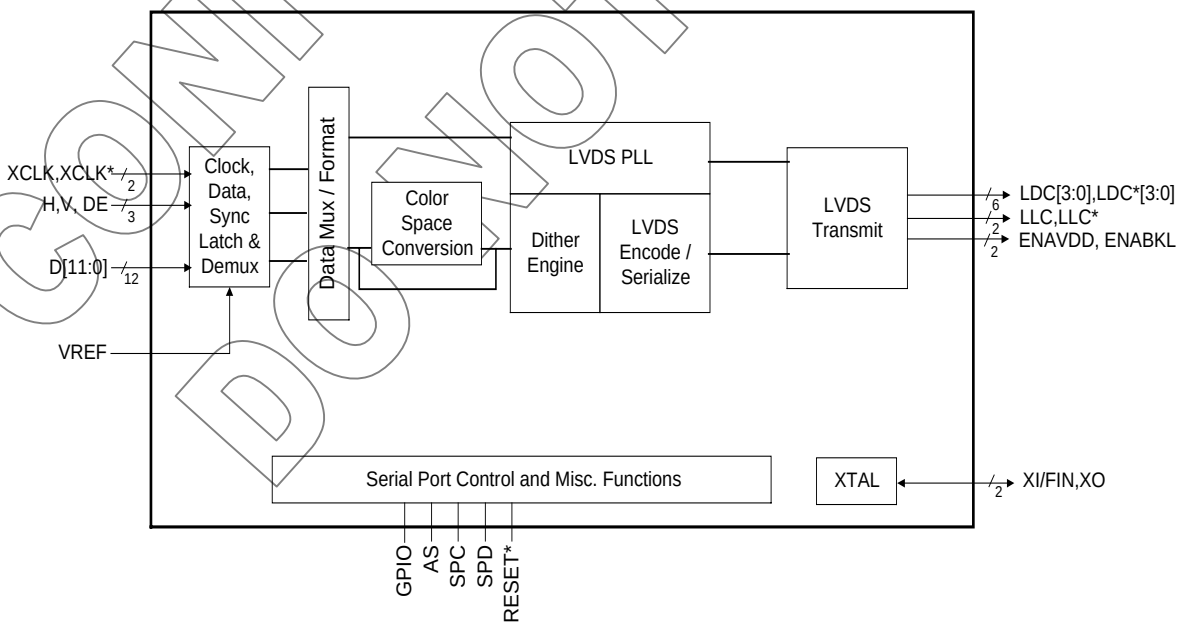

Figure 1: Functional Block Diagram

2.0 Pin Assignment

2.1 Package Diagram

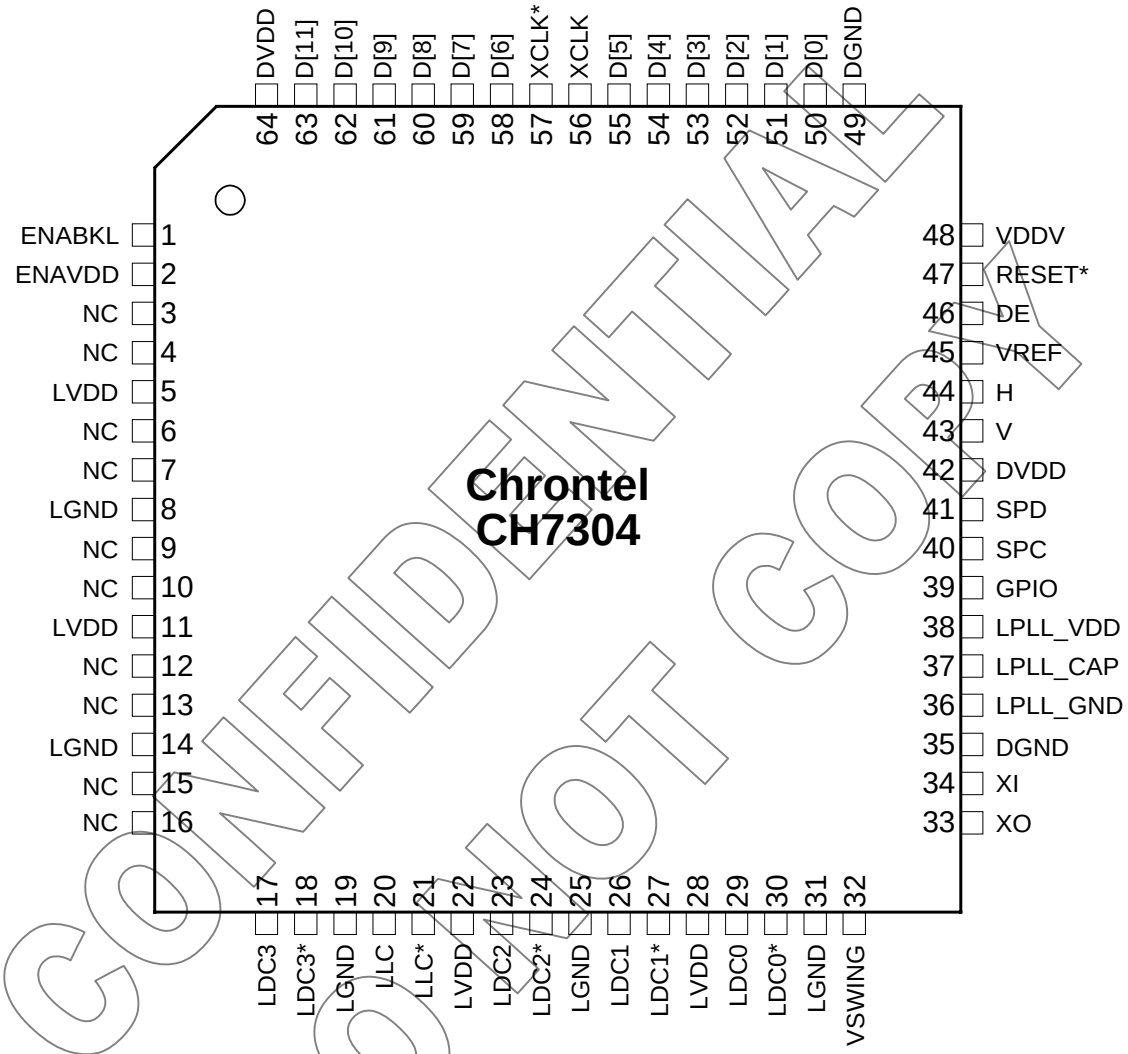

Figure 2: 64 Pin LQFP Package (Top View)

2.2 Pin Description

Table 1: Pin Description

Pin #	# of Pins	Type	Symbol	Description
1	1	Out	ENABLK	**Back Light Enable** Enable Back-Light of LCD Panel. Output is driven from 0 to DVDD.
2	1	Out	ENAVDD	**Panel Power Enable** Enable panel VDD. Output is driven from 0 to DVDD.
3,4,6,7,9,10, 12,13,15,16	10	-	NC	**No Connect**
20, 21	2	Out	LLC, LLC*	**LVDS Differential Clock**
17,23,26,29	4	Out	LDC[3:0]	**Positive LVDS differential data[3:0]**
18,24,27,30	4	Out	LDC[3:0]*	**Negative LVDS differential data [3:0]**
32	1	In	VSWING	**LVDS Voltage Swing Control** This pin sets the swing level of the LVDS outputs. A 2.4K Ohm resistor should be connected between this pin and LGND (pin 31) using short and wide traces.
33	1	Out	XO	**Crystal Output** A parallel resonance 14.31818MHz crystal (± 20 ppm) should be attached between this pin and XI. However, if an external CMOS clock is attached to XI, XO should be left open.
34	1	In	XI	**Crystal Input / External Reference Input** A parallel resonance 14.31818MHz crystal (± 20 ppm) should be attached between this pin and XO. However, an external CMOS compatible clock can drive the XI input.
37	1	Analog	LPLL_CAP	**LVDS PLL Capacitor** This pin allows coupling of any signal to the on-chip loop filter capacitor.
39	1	In/Out	GPIO	**General Purpose Input / Output** This pin provides general purpose I/O and is controlled via the serial port. The voltage level on input and output is DVDD. See description of GPIO Controls for I/O configuration.
40	1	In	SPC	**Serial Port Clock Input** This pin functions as the clock input of the serial port and can operate with inputs from 1.1V ~ 3.3V.
41	1	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port and can operate with inputs from 1.1V ~ 3.3V. Outputs are driven from 0 to VDDV.
43	1	In	V	**Vertical Sync Input** This pin accepts a vertical sync input for use with the input data. The amplitude will be 0 to VDDV. VREF signal is the threshold level.
44	1	In	H	**Horizontal Sync Input** This pin accepts a horizontal sync input for use with the input data. The amplitude will be 0 to VDDV. VREF is the threshold level for this input.
45	1	In	VREF	**Reference Voltage Input** The VREF pin inputs a reference voltage of VDDV / 2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, sync and clock inputs.
46	1	In	DE	**Data Enable** This pin accepts a data enable signal which is high when active video data is input to the device, and remains low during all other times. The levels are 0 to VDDV. VREF is the threshold level.

Table 1: Pin Description (continued)

Pin #	# of Pins	Type	Symbol	Description
47	1	In	RESET*	**Reset * Input** (Internal Pull-up) When this pin is low, the device is held in the power on reset condition. When this pin is high, reset is controlled through the serial port.
50-55, 58-63	12	In	D [11:0]	**Data[11] through Data[0] Inputs** These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to VDDV. VREF is the threshold level.
57, 56	2	In	XCLK, XCLK*	**External Clock Inputs** These inputs form a differential clock signal input to the device for use with the H, V and D[11:0] data. If differential clocks are not available, the XCLK* input should be connected to VREF. The clock polarity can be selected by the MCP control bit **(Register 1Ch)**.
42, 64	2	Power	DVDD	**Digital Supply Voltage** (3.3V)
35, 49	2	Power	DGND	**Digital Ground**
48	1	Power	VDDV	**I/O Supply Voltage** (1.1V to 3.3V)
5,11,22,28	4	Power	LVDD	**LVDS Supply Voltage** (3.3V)
8,14,19,25,31	5	Power	LGND	**LVDS Ground**
38	1	Power	LPLL_VDD	**LVDS PLL Supply Voltage** (3.3V)
36	1	Power	LPLL_GND	**LVDS PLL Ground**

3.0 Electrical Specifications

3.1 Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	All power supplies relative to GND	-0.5		5.0	V
	Input voltage of all digital pins	GND – 0.5		VDD + 0.5	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature	0		85	°C
T_{STOR}	Storage temperature	-65		150	°C
T_J	Junction temperature			150	°C
T_{VPS}	Vapor phase soldering (1 minute)			220	°C

Note:

1) Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2) The device is fabricated using high-performance CMOS technology. It should be handled as an ESD sensitive device. Voltage on any signal pin that exceeds the power supply voltages by more than ± 0.5V can induce destructive latchup.

3.2 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
LPLL_VDD	LVDS PLL Power Supply Voltage	3.1	3.3	3.6	V
DVDD	Digital Power Supply Voltage	3.1	3.3	3.6	V
LVDD	LVDS Power Supply Voltage	3.1	3.3	3.6	V
VDD	Generic for all of the above supplies	3.1	3.3	3.6	V
VDDV	I/O Power Supply Voltage	1.1	1.8	3.6	V

3.3 Electrical Characteristics (Operating Conditions: T_A = 0°C – 70°C, VDD =3.3V ± 5%)

Symbol	Description	Min	Typ	Max	Units
I_{VDD}	Total supply current 1 DVO input for LVDS@165 MHz LVDS output @ 165 MHz		TBD		mA
I_{VDD}	Total supply current 1 DVO input for LVDS@80 MHz LVDS output @ 80 MHz		TBD		mA
I_{VDDV}	VDDV (1.8V) current (15pF load)		4		mA
I_{PD}	Total Power Down Current		0.01	0.1	mA

3.4 Digital Inputs / Outputs

Symbol	Description	Test Condition	Min	Typ	Max	Unit
V_{SDOL}	SPD (serial port data) Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{SPIH}	Serial Port (SPC, SPD) Input High Voltage		1.0		VDD + 0.5	V
V_{SPIL}	Serial Port (SPC, SPD) Input Low Voltage		GND-0.5		0.4	V
V_{HYS}	Hysteresis of Inputs		0.25			V
V_{DATAIH}	D[11:0] Input High Voltage		Vref+0.25		DVDD+0.5	V
V_{DATAIL}	D[11:0] Input Low Voltage		GND-0.5		Vref-0.25	V
$V_{MISCAIH}$	GPIO, RESET* Input High Voltage	DVDD=3.3V	2.7		VDD + 0.5	V
$V_{MISCAIL}$	GPIO, RESET* Input Low Voltage	DVDD=3.3V	GND-0.5		0.6	V
$I_{MISCAPU}$	Pull Up Current (GPIO, RESET*)	V_{IN} = 0V	0.5		5	uA
$V_{MISCAOH}$	GPIO, ENAVDD, ENABKL, Output High Voltage	I_{OH} = -0.4mA	VDD-0.2			V
$V_{MISCAOL}$	GPIO, ENAVDD, ENABKL, Output Low Voltage	I_{OL} = 3.2mA			0.2	V

3.5 AC Specifications

Symbol	Description	Test Condition	Min	Typ	Max	Unit
f_{XCLK}	Input (XCLK) frequency		25		165	MHz
t_{PIXEL}	Pixel time period		6.06		40	ns
DC_{XCLK}	Input (XCLK) Duty Cycle	$T_S + T_H < 1.2$ns	30		70	%
t_{XJIT}	XCLK clock jitter tolerance			2		ns
t_S	Setup Time: D[11:0], H, V and DE to XCLK, XCLK*	XCLK = XCLK* to D[11:0], H, V, DE = Vref	0.5			ns
t_H	Hold Time: D[11:0], H, V and DE to XCLK, XCLK*	D[11:0], H, V, DE = Vref to XCLK = XCLK*	0.5			ns
t_{STEP}	De-skew time increment		50		80	ps

4.0 Package Dimensions

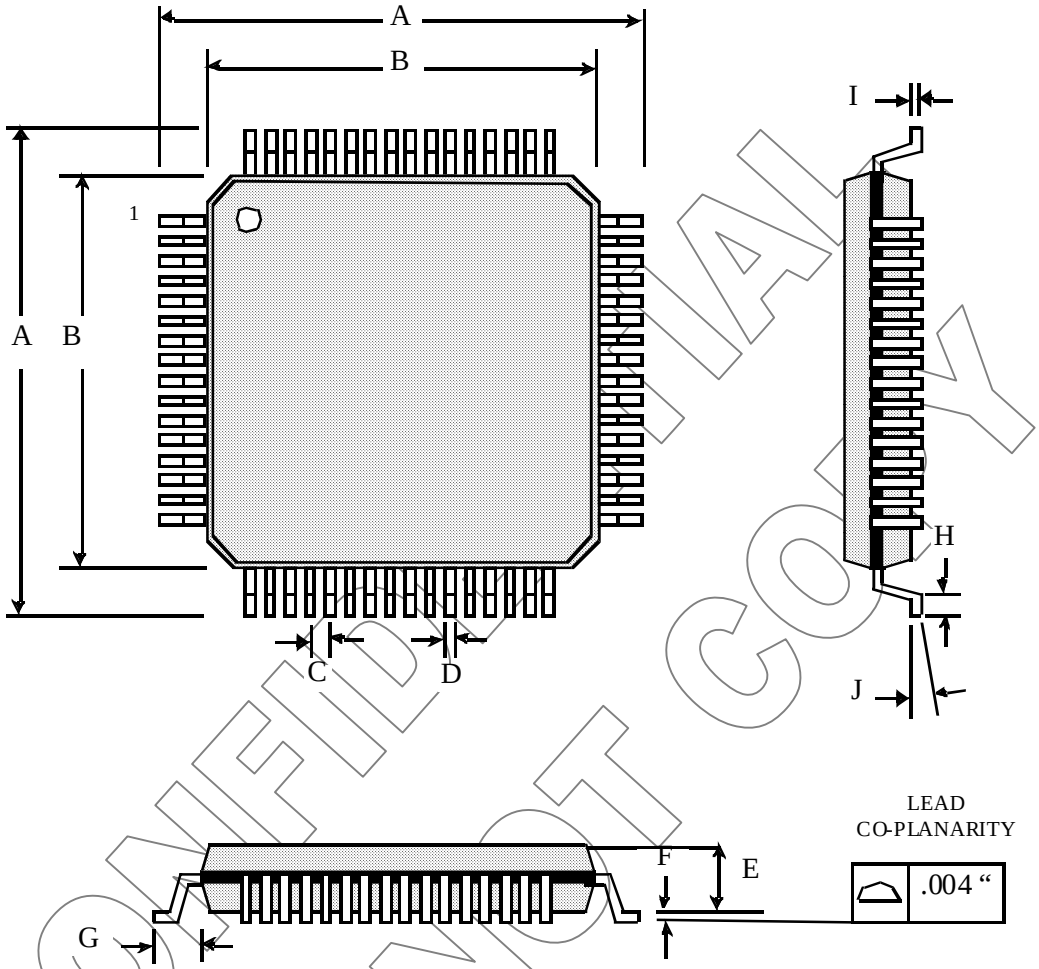

Table of Dimensions

No. of Leads		SYMBOL									
64 (10 X 10 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	12	10	0.50	0.17	1.35	0.05	1.00	0.45	0.09	0°
	MAX				0.27	1.45	0.15		0.75	0.20	7°

Figure 3: 64 Pin LQFP Package

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