Chrontel CH7305 LVDS Transmitter

Features

- Single / Dual LVDS transmitter
- Supports pixel rate up to 165Mpixels/sec
- LVDS low jitter PLL
- LVDS 24-bit or 18-bit output
- 2D dither engine
- Panel protection and power down sequencing
- Programmable power management
- Fully programmable through serial port
- Complete Windows and DOS driver support
- Variable voltage interface to graphics device
- Offered in a 64-pin LQFP package

General Description

The CH7305 is a Display Controller device, which accepts a graphics data stream over one 12-bit wide variable voltage ports. The data stream outputs through an LVDS transmitter to an LCD panel. A maximum of 165M pixels per second can be output through a single or dual LVDS link.

The LVDS transmitter supports 24-bit panels; it also includes a programmable dither function for support of 18-bit panels. Data is encoded into commonly used formats, including those detailed in the OpenLDI and the SPWG specifications. Serialized data outputs on four to eight differential channels.

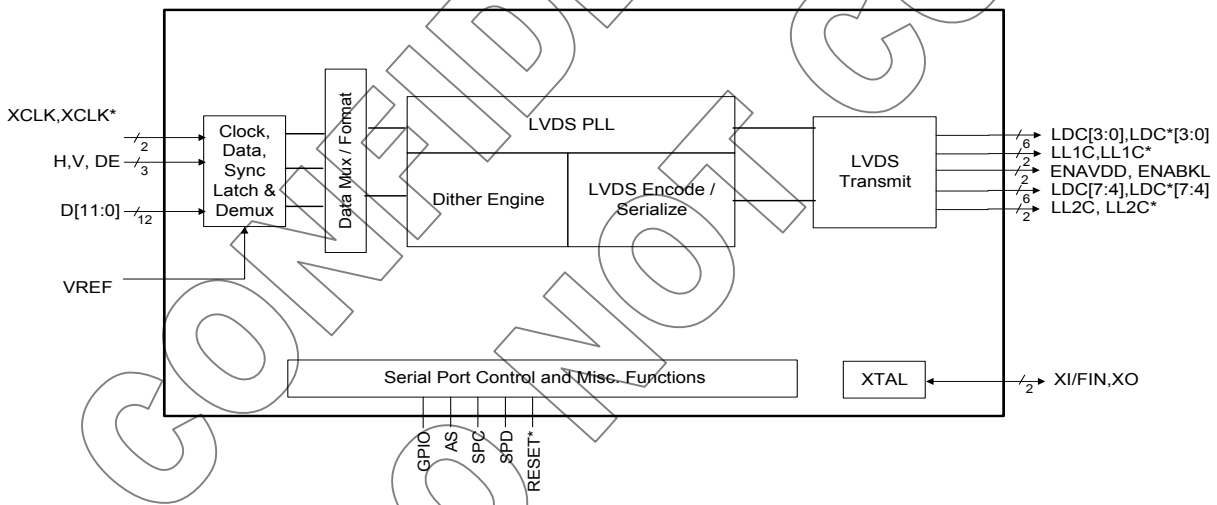

Figure 1: Functional Block Diagram

1.0 Pin Assignment

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1.1 Package Diagram

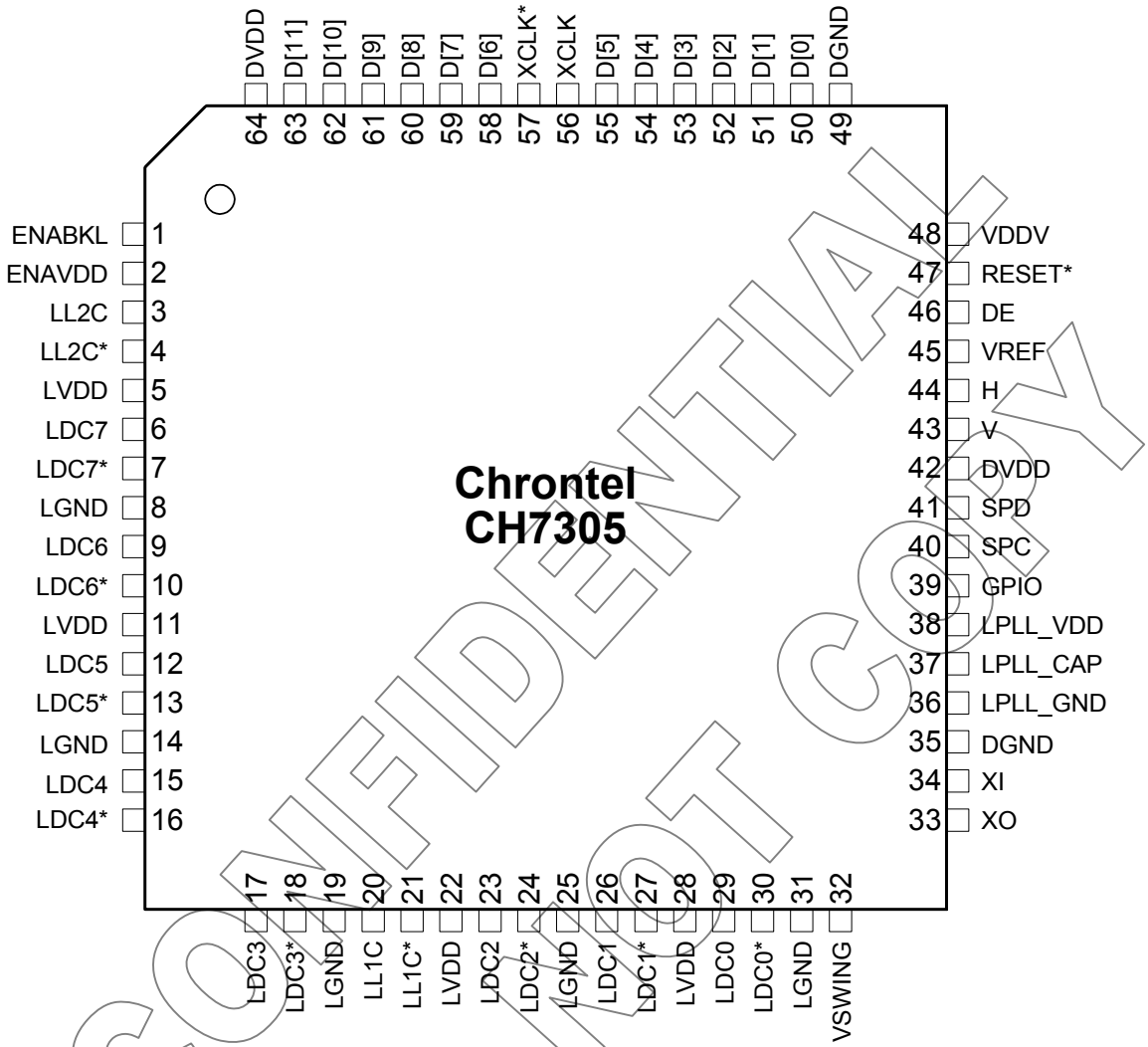

Figure 2: 64 Pin LQFP Package (Top View)

1.2 Pin Description

Table 1: Pin Description

Pin #	# of Pins	Type	Symbol	Description
1	1	Out	ENABLK	**Back Light Enable** Enable Back-Light of LCD Panel. Output is driven from 0 to DVDD.
2	1	Out	ENAVDD	**Panel Power Enable** Enable panel VDD. Output is driven from 0 to DVDD.
3, 4	2	Out	LL2C, LL2C*	**LVDS Differential Clock – channel 2**
6,9,12,15	4	Out	LDC[7:4]	**Positive LVDS differential data[7:4] – channel 2**
7,10,13,16	4	Out	LDC[7:4]*	**Negative LVDS differential data[7:4] – channel 2**
20, 21	2	Out	LL1C, LL1C*	**LVDS Differential Clock – channel 1**
17,23,26,29	4	Out	LDC[3:0]	**Positive LVDS differential data[3:0] – channel 1**
18,24,27,30	4	Out	LDC[3:0]*	**Negative LVDS differential data [3:0] – channel 1**
32	1	In	VSWING	**LVDS Voltage Swing Control** This pin sets the swing level of the LVDS outputs. A 2.4K Ohm resistor should be connected between this pin and LGND (pin 20) using short and wide traces.
33	1	Out	XO	**Crystal Output** A parallel resonance 14.31818MHz crystal (± 20 ppm) should be attached between this pin and XI. However, if an external CMOS clock is attached to XI, XO should be left open.
34	1	In	XI	**Crystal Input / External Reference Input** A parallel resonant 14.31818MHz crystal (± 20 ppm) should be attached between this pin and XO. However, an external CMOS compatible clock can drive the XI input.
37	1	Analog	LPLL_CAP	**LVDS PLL Capacitor** This pins allows coupling of any signal to the on-chip loop filter capacitor.
39	1	In/Out	GPIO	**General Purpose Input / Output** This pin provides general purpose I/O and is controlled via the serial port. The voltage level on input and output is DVDD. See description of GPIO Controls for I/O configuration.
40	1	In	SPC	**Serial Port Clock Input** This pin functions as the clock input of the serial port and can operate with inputs from VDDV to DVDD.
41	1	In/Out	SPD	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port and can operate with inputs from VDDV to DVDD. Outputs are driven from 0 to VDDV.
43	1	In	V	**Vertical Sync Input** This pin accepts a vertical sync inputs for use with the input data. The amplitude will be 0 to VDDV. VREF signal is the threshold level.
44	1	In	H	**Horizontal Sync Input** This pin accepts a horizontal sync inputs for use with the input data. The amplitude will be 0 to VDDV. VREF is the threshold level for these inputs.
45	1	In	VREF	**Reference Voltage Input** The VREF pin inputs a reference voltage of VDDV / 2. The signal is derived externally through a resistor divider and decoupling capacitor, and will be used as a reference level for data, sync and clock inputs.
46	1	In	DE	**Data Enable** These pins accept a data enable signal which is high when active video data is input to the device, and remains low during all other times. The levels are 0 to VDDV. VREF is the threshold level.
47	1	In	RESET*	**Reset * Input** (Internal Pull-up) When this pin is low, the device is held in the power on reset condition. When this pin is high, reset is controlled through the serial port.

Table 1: Pin Description (continued)

Pin #	# of Pins	Type	Symbol	Description
50-55, 58-63	12	In	D1[11:0]	**Data[11] through Data[0] Inputs** These pins accept the 12 data inputs from a digital video port of a graphics controller. The levels are 0 to VDDV. VREF is the threshold level.
57, 56	2	In	XCLK, XCLK*	**External Clock Inputs** These inputs form a differential clock signal input to the device for use with the H, V and D[11:0] data. If differential clocks are not available, the XCLK* input should be connected to VREF. The clock polarity can be selected by the MCP control bit (register 1Ch).
42, 64	2	Power	DVDD	**Digital Supply Voltage** (3.3V)
35, 49	2	Power	DGND	**Digital Ground**
48	1	Power	VDDV	**I/O Supply Voltage** (1.1V to 3.3V)
5,11,22,28	5	Power	LVDD	**LVDS Supply Voltage** (3.3V)
8,14,19,25,31	5	Power	LGND	**LVDS Ground**
38	1	Power	LPLL_VDD	**LVDS PLL Supply Voltage** (3.3V)
36	1	Power	LPLL_GND	**LVDS PLL Ground**

4.0 Package Dimensions

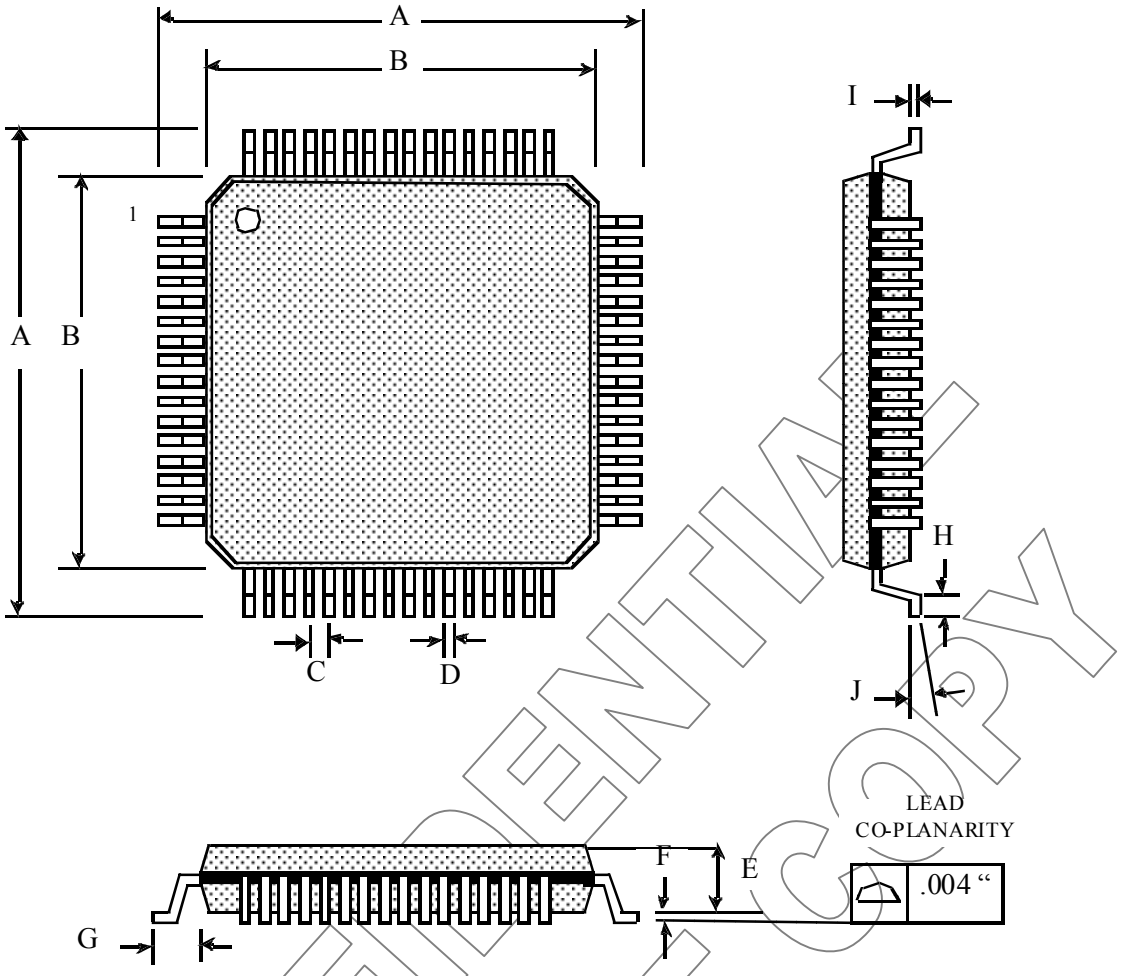

Table of Dimensions

No. of Leads		SYMBOL									
64 (10 X 10 mm)		A	B	C	D	E	F	G	H	I	J
Milli-meters	MIN	12	10	0.50	0.17	1.35	0.05	1.00	0.45	0.09	0°
	MAX				0.27	1.45	0.15		0.75	0.20	7°

Figure 8: 64 Pin LQFP Package

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